

The Atari Historical Society
www.atari-history.com

POKEY
COL2294

CONFIDENTIAL

REVISIONS				DRAWN BY: <i>R. J.</i> DATE: <i>3-9-82</i>	 ATARI INCORPORATED 1265 BORREGAS AVE. SUNNYVALE, CA. 94086		
SYM	DESCRIPTION	DATE	APPV'D	CHECKED: <i>[Signature]</i> DATE: <i>3/15/82</i>			
B	RELEASE PER ECN 5320	3-30-82	<i>EW</i>	ENGINEER <i>J. E. Longwater</i> 3/15/82 ENGINEER, MGR. QUALITY ASSURANCE MFG. ENGINEER	TITLE POKEY CHIP		
					SIZE A	DRAWING NO. COL2294	REV B
					SCALE -		SHEET 1 OF 41

TABLE OF CONTENTS:

1. GENERAL DESCRIPTION	page 3
2. AUDIO	page 3
3. KEYBOARD SCAN	page 10
4. POT PORTS	page 15
5. TIMERS	page 17
6. RANDOM NUMBER GENERATOR	page 17
7. SERIAL I/O PORT	page 18
8. IRQ INTERRUPTS	page 23
9. ELECTRICAL PARAMETERS	page 25
A. GENERAL	page 25
B. D.C. AND OPERATING CHARACTERISTICS	page 25
C. DYNAMIC OPERATING CHARACTERISTICS	page 28
D. WRITE I/O TIMING	page 29
E. READ I/O TIMING	page 30
F. MISC. I/O TIMING	page 31

TABLE OF ILLUSTRATIONS:

1. AUDIO NOISE FILTERS	pages 5 & 6
2. MUSICAL NOTE TABLE	page 9
3. KEY SCAN FLOW CHART	page 11
4. TYPICAL KEYBOARD CONFIGURATION	page 12
5. KEY SCAN LINE TIMING	page 13
6. INTERNAL KEY SCAN LOGIC (BLOCK DIAGRAM).....	page 14
7. INTERNAL POT PORT LOGIC (BLOCK DIAGRAM).....	page 16
8. POKEY ADDRESS TABLE	page 32
9. POKEY PIN LIST	page 33
10. POKEY BONDING DIAGRAM.....	page 34
11. POKEY MOS LOGIC.....	pages 35 - 41



TITLE

POKEY CHIP

DRAWING NO C012294

REV B

SHEET 2

OF 4

1. GENERAL DESCRIPTION:

There are four semi-independent audio channels, each with its own frequency, noise and volume control. Each channel has an eight bit "divide by N" frequency divider and an eight bit control register, which selects the noise (polynomial counter) content and volume.

There are six key scan lines (K0-K5), which holds a value from 00 to 3F. There are two sense lines. One of the sense lines is for the full decode of the six scan lines. The other sense line is for decoding only the codes (CTRL, SHIFT, and BREAK-key).

There are eight pot ports for measuring input rise time. Each input has an eight bit counter which is clocked every TV line. Each input also has a dump transistor which is turned on or off by software.

There are three timers which use the audio channels. If start timer (STIMER) is enabled, the audio channels are reset.

There is a random number generator which is eight bits from a polynomial counter.

There is a serial I/O port. The serial port consists of a serial output line, a serial input line, a serial output clock line, and a bi-directional serial data clock line. Also there are control registers which are used to configure the serial port.

There are eight IRQ interrupts. They are BREAK key, OTHER key, SERIAL INPUT READY, SERIAL OUTPUT NEEDED, TRANSMISSION FINISHED, TIMER #4, TIMER #2, and TIMER #1. These interrupts can be enabled or disabled by software. There is also a register to read interrupt status.

2. AUDIO:

There are four semi-independent audio channels, each with its own frequency, noise, and volume control. Each channel has an eight bit "divide by N" frequency divider, controlled by an eight bit register (AUDFX). Each channel also has an eight bit control register (AUDCX) which selects the noise (polynomial counter) content and the volume.

All four frequency dividers can be clocked simultaneously from 64 KHZ or 15 KHZ by AUDCTL bit 0. Frequency dividers 1 and 3 can alternately be clocked from



TITLE

POKEY CHIP

DRAWING NO.

CO12294

REV

B

SHEET

3

OF

4

2. AUDIO (continued)

1.79 MHZ by setting AUDCTL bits 5 and 6. Frequency dividers 2 and 4 can alternately be clocked with the output of dividers 1 and 3 by setting AUDCTL bits 4 and

3. This allows the following options: 4 channels of 8 bit resolution, 2 channels of 16 bit resolution, or 1 channel of 16 bit resolution and 2 channels of 8 bit resolution.

There are three polynomial counters (17 bit, 5 bit and 4 bit) used to generate random noise. The 17 bit poly counter can be reduced to a 9 bit poly counter by bit 7 of AUDCTL. These counters are clocked by 1.79 MHZ. Their outputs, however, can be sampled independently by the four audio channels at a rate determined by each channel's frequency divider. Thus each channel appears to contain separate poly counters clocked at its own frequency. This poly counter noise sampling is controlled by bits 5, 6, and 7 of each AUDCX register. Because the poly counters are sampled by the "divide by N" frequency divider, the output obviously cannot change faster than the sampling rate. In these modes (poly noise outputted), the dividers are therefore acting as "low pass" filter clocks, allowing only the low frequency noise to pass.

The output of the noise control circuit described above consists of pure tones (square wave type), or polynomial counter noise at a maximum frequency set by the "divide by N" counter (low pass clock). This output can be routed through a high pass filter if desired by use of bits 1 and 2 of AUDCTL.

The high pass filter consists of a "D" flip flop and an exclusive-OR Gate. The noise control circuit output is sampled by this flip flop at a rate set by the "High Pass" clock. The input and output of the Flip Flop pass through the exclusive-OR Gate. However, if it is lower than the clock rate, the flip flop output will tend to follow the input and the two exclusive-OR Gate inputs will mostly be identical (11 or 00) giving very little output. This gives the effect of a crude high pass filter, passing noise whose minimum frequency is set by the high pass clock rate. Only channels 1 and 2 have such a high pass filter. The high pass clock for channel 1 comes from the channel 3 divider. The high pass clock for channel 2 comes from the channel 4 divider. This filter is included only if bit 1 or 2 of AUDCTL is true.

A volume control circuit is placed at the output of each channel. This is a crude 4 bit digital to analog converter that allows selection of one of 16 possible output current levels for a logic true audio input. A logic zero audio input to this volume circuit always gives an open circuit (zero current) output. The volume selection is controlled by bits 0 through 3 of AUDCX. "Volume Control only" mode



TITLE

POKEY CHIP

DRAWING NO.

COL2294

REV B

SHEET

4

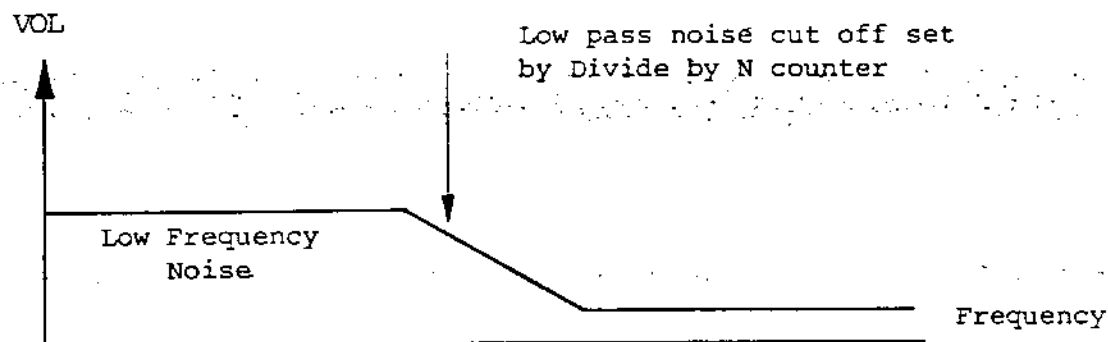
OF 41

2. AUDIO (continued)

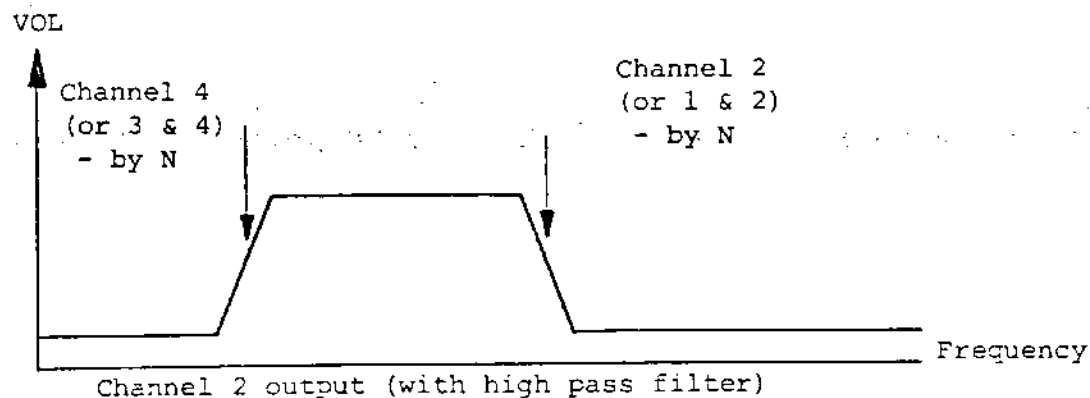
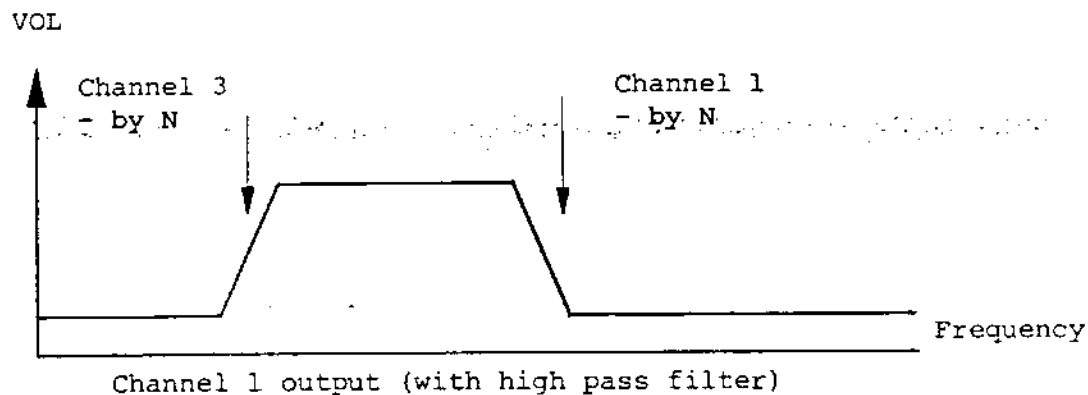
can be invoked by forcing this circuit's audio input true with bit 4 of AUDCX. In this mode the dividers, noise counters, and filter circuits are all disconnected from the channel output. Only the volume control bits (0 to 3 of AUDCX) determine the channel output current.

The audio output of any channel can be completely turned off by writing zero to the volume control bits of AUDCX. All ones give maximum volume.

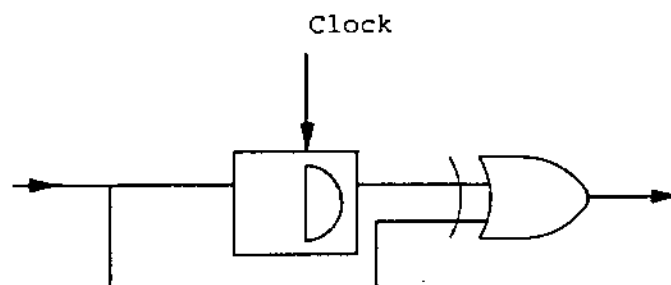
AUDIO NOISE FILTERS:



Any channel noise output (without high pass filter)



AUDIO NOISE FILTERS (continued):



AUDCTL (Audio Control) (08): This address writes data into the Audio Mode Control Register. (Also see SKCTL two-tone bit 3 and notes).

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

- D7 Change 17 bit poly into a 9 bit below poly.
- D6 Clock Channel 1 with 1.79 MHZ, instead of 64 KHZ.
- D5 Clock Channel 3 with 1.79 MHZ, instead of 64 KHZ.
- D4 Clock Channel 2 with Channel 1, instead of 64 KHZ (16 BIT).
- D3 Clock Channel 4 with Channel 3, instead of 64 KHZ (16 BIT).
- D2 Insert Hi Pass Filter in Channel 1, clocked by Channel 3.
(See section II.)
- D1 Insert Hi Pass Filter in Channel 2, clocked by Channel 4.
- D0 Change Normal 64 KHZ frequency, into 15 KHZ.

Exact Frequencies: The frequencies given above are approximate. The Exact Frequency (F_{in}) that clocks the divide by N counters is given below (NTSC only, PAL different).

F_{in} (Approximate)	F_{in} (Exact)	
1.79 MHZ	1.78979 MHZ	- Use modified formula for F_{out}
64 KHZ	63.9210 KHZ	
15 KHZ	15.6999 KHZ	- Use normal formula for F_{out}



TITLE

POKEY CHIP

DRAWING NO.

002294

REV

B

SHEET

6

OF 4

The Normal Formula for output frequency is:

$$F_{out} = F_{in}/2N$$

Where N = the binary number in the frequency register (AUDF), plus 1 (N=AUDF+1).

The MODIFIED FORMULA should be used when $F_{in} = 1.79 \text{ MHz}$ and a more exact result is desired:

$$F_{out} = \frac{F_{in}}{2(AUDF + M)}$$

Where: M = 4 if 8 bit counter (AUDCTL bit 3 or 4 = 0)

M = 7 if 16 bit counter (AUDCTL bit 3 or 4 = 1)

AUDF1, AUDF2, AUDF3, AUDF4, (Audio Frequency) (00, 02, 04, 06):

These addresses write data into each of the four Audio Frequency Control Registers.

Each register controls a divide by "N" counter.

D7	D6	D5	D4	D3	D2	D1	D0	"N"
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
ETC.								
1	1	1	1	1	1	1	1	256

Note: "N" is one greater than the binary number in Audio Frequency Register AUDF(X).

AUDC1, AUDC2, AUDC3, AUDC4 (Audio Channel Control) (01, 03, 05, 07):

These addresses write data into each of the four Audio Control Registers. Each Register controls the noise content and volume of the corresponding Audio Channel.

Noise Content or Distortion					Volume				
HEX	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0					Divisor "N" set by audio frequency register. - 17 BIT poly - 5 BIT poly - N - 5 BIT poly - N - 2 - 4 BIT poly - 5 BIT poly - N - 5 BIT poly - N - 2 - 17 BIT poly - N - Pure Tone - N - 2 - 4 BIT poly - N
2	0	0	1	0					
4	0	1	0	0					
6	0	1	1	0					
8	1	0	0	0					
A	1	X	1	0					
C	1	1	0	0					
1	X	X	X	1					- Force Output (Volume only)
0					0	0	0	0	- Lowest Volume (Off)
8					1	0	0	0	- Half Volume
F					1	1	1	1	- Highest Volume

MUSICAL NOTE TABLE

PITCH VALUES FOR THE MUSICAL NOTES-AUDCTL =0, AUDC = hex AX

		Hex	AUDF	Dec
HIGH NOTES	C	1D		29
	B	1F		31
	A# or Bb	21		33
	A	23		35
	G# or Ab	25		37
	G	28		40
	F# or Gb	2A		42
	F	2D		45
	E	2F		47
	D# or Eb	32		50
	D	35		53
	C# or Db	39		57
	C	3C		60
	B	4G		64
	A# or Bb	44		68
	A	48		72
MIDDLE C	G# or Ab	4C		76
	G	51		81
	F# or Gb	55		85
	F	5B		91
	E	60		96
	D# or Eb	66		102
	D	6C		108
	C# or Db	72		114
	C	79		121
	B	80		128
	A# or Bb	88		136
	A	90		144
	G# or Ab	99		153
	G	A2		162
	F# or Gb	AD		173
	F	B6		182
LOW : NOTES	E	C1		193
	D# or Eb	CC		204
	D	D9		217
	C# or Db	E6		230
	C	F3		243

3. KEYBOARD SCAN:

The $\overline{K0-K5}$ lines hold a 6 bit value from 00 to 3 F. This allows for decoding 64 keys. With external CMOS (4052) chips, a key matrix is formed. The value of the key selected by the key matrix is returned on the $\overline{KR1}$ line.

Internal to the Pokey is a 6 bit binary counter, a 6 bit compare latch, and an 8 bit keycode latch. A control state machine does debouncing of the keys.

When the keyboard scanner is enabled by the SKCTL register, the binary counter begins to count, once per line. If the $\overline{KR1}$ line goes low, the value of the binary counter is transferred to compare latch. This will be the key code to be debounced. If $\overline{KR1}$ goes low before the next time the binary counter equals the compare latch then there are two keys depressed and both are ignored. If the binary counter equals the compare latch and $\overline{KR1}$ is high, then the key is bouncing and is ignored, but if $\overline{KR1}$ is low then the key is valid and it is transferred to the keycode latch for reading by the CPU. An IRQ is also sent indicating the key is ready. As soon as $\overline{KR1}$ is low and the binary counter equals compare latch, the key is still depressed. As soon as $\overline{KR1}$ is high, then the key will be checked for debounce. The next time the binary counter equals the compare latch and $\overline{KR1}$ is high, then the key is debounced and another key can be looked for. But if $\overline{KR1}$ is low, then the key is bouncing and is assumed to be still pressed.

If the debounce is disabled, the Pokey forces the binary counter equal compare latch signal to a logic true value which will disable debounce.

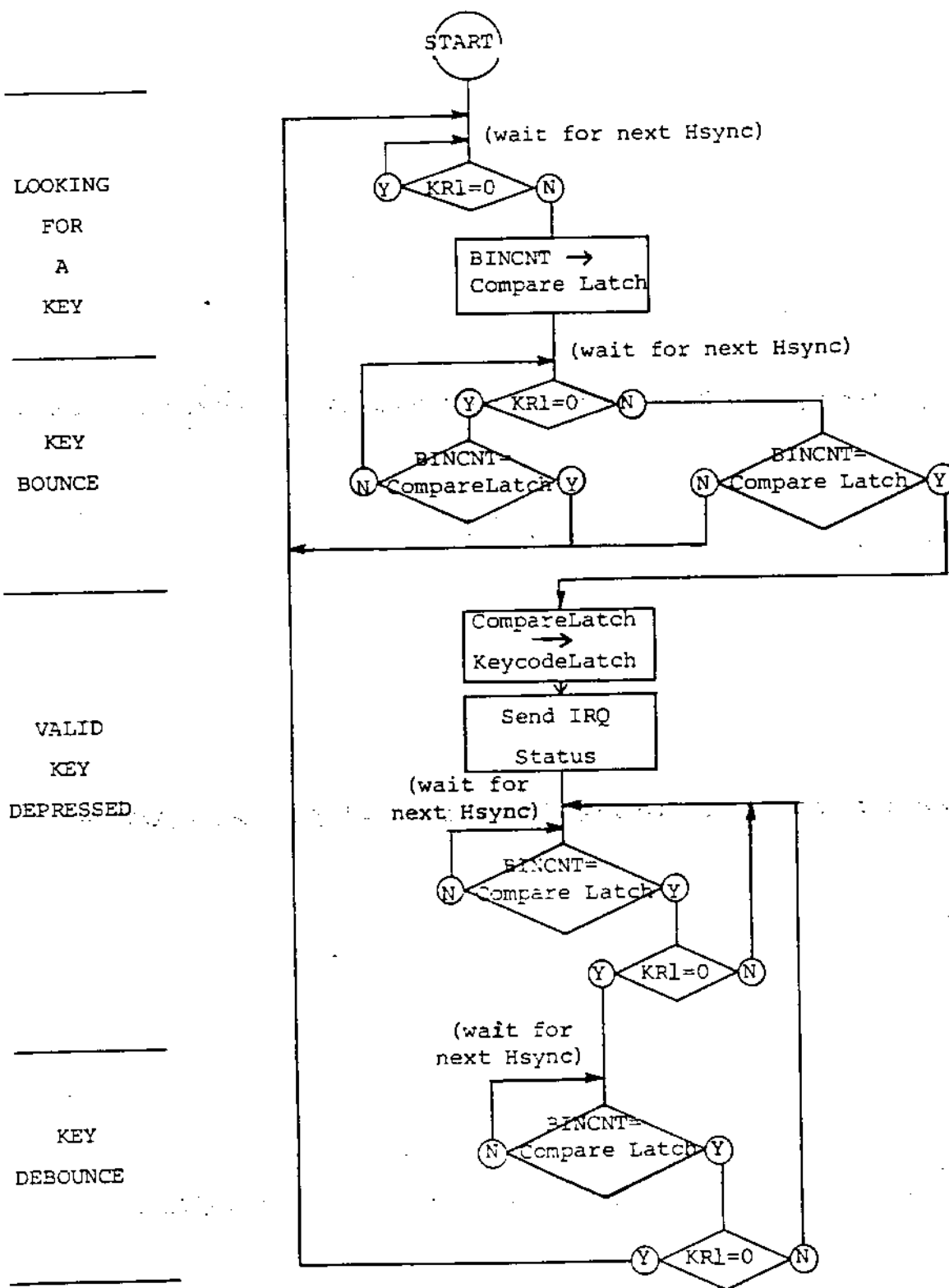
$\overline{KR2}$ input is used to decode 3 keys. They are SHIFT, BREAK and CONTROL. They do not get debounced. They are decoded only at:

	$\overline{K0}$	$\overline{K1}$	$\overline{K2}$	$\overline{K3}$	$\overline{K4}$	$\overline{K5}$
BREAK	= 1	1	1	1	0	0
SHIFT	= 1	1	1	1	0	1
CONTROL	= 1	1	1	1	1	1

KBCODE (Keyboard Code) (09): This address reads the Keyboard Code, and is usually read in response to a Keyboard Interrupt (IRQ and bits 6 or 7 of IRQST). See IRQEN for information on enabling keyboard interrupts. See SKCTL bits 1 and 0 for key scan and debounce enable.

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

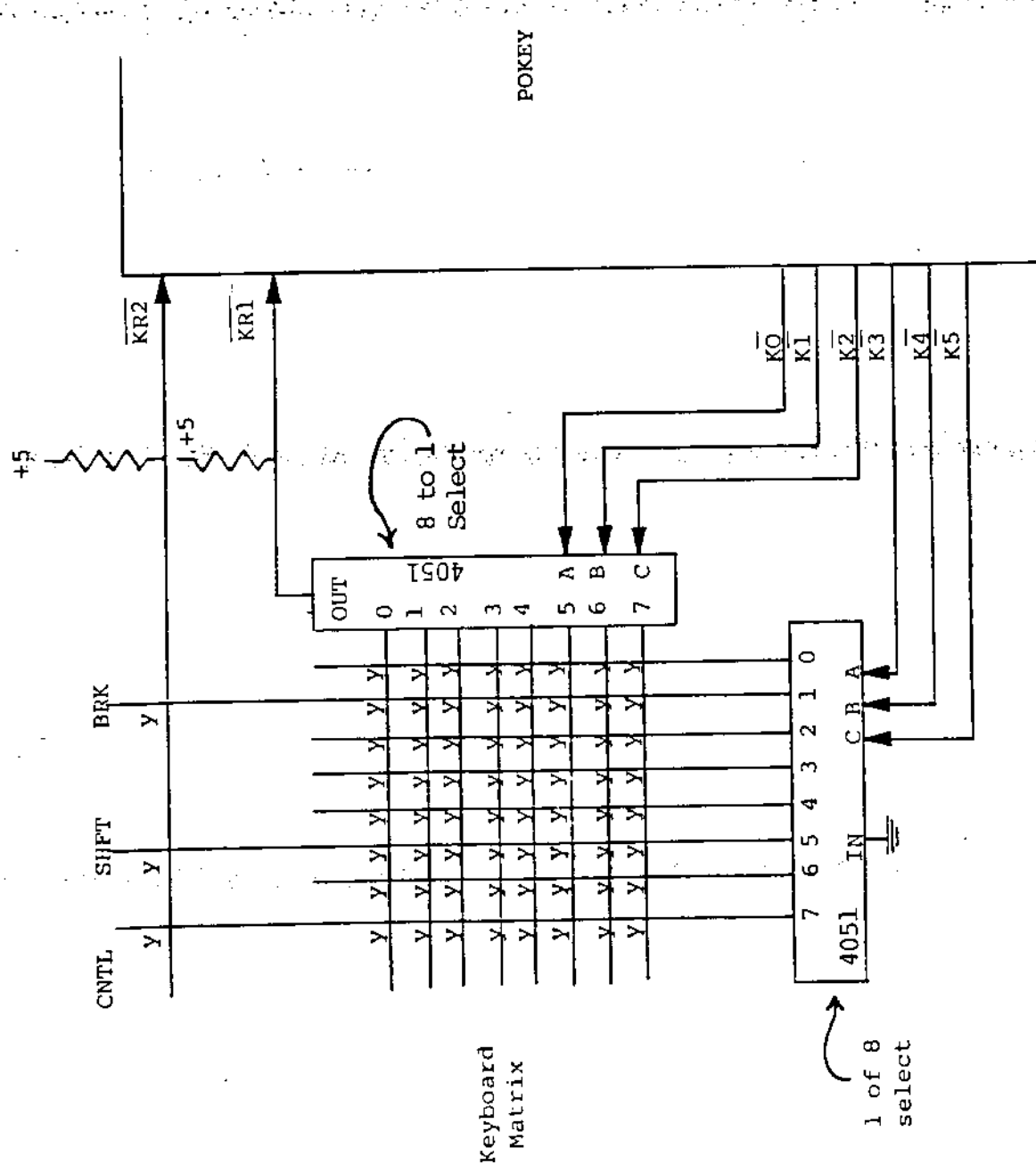
D7 = Control Key
D6 = Shift Key



If Debounce Disable is in effect
then BINCNT = Compare Latch

POKEY KEYBOARD SCAN

	K0	K1	K2	K3	K4	K5
CNTL	1	1	1	1	1	1
SHIFT	1	1	1	1	0	1
BRK	1	1	1	1	0	0



ATARI

TITLE

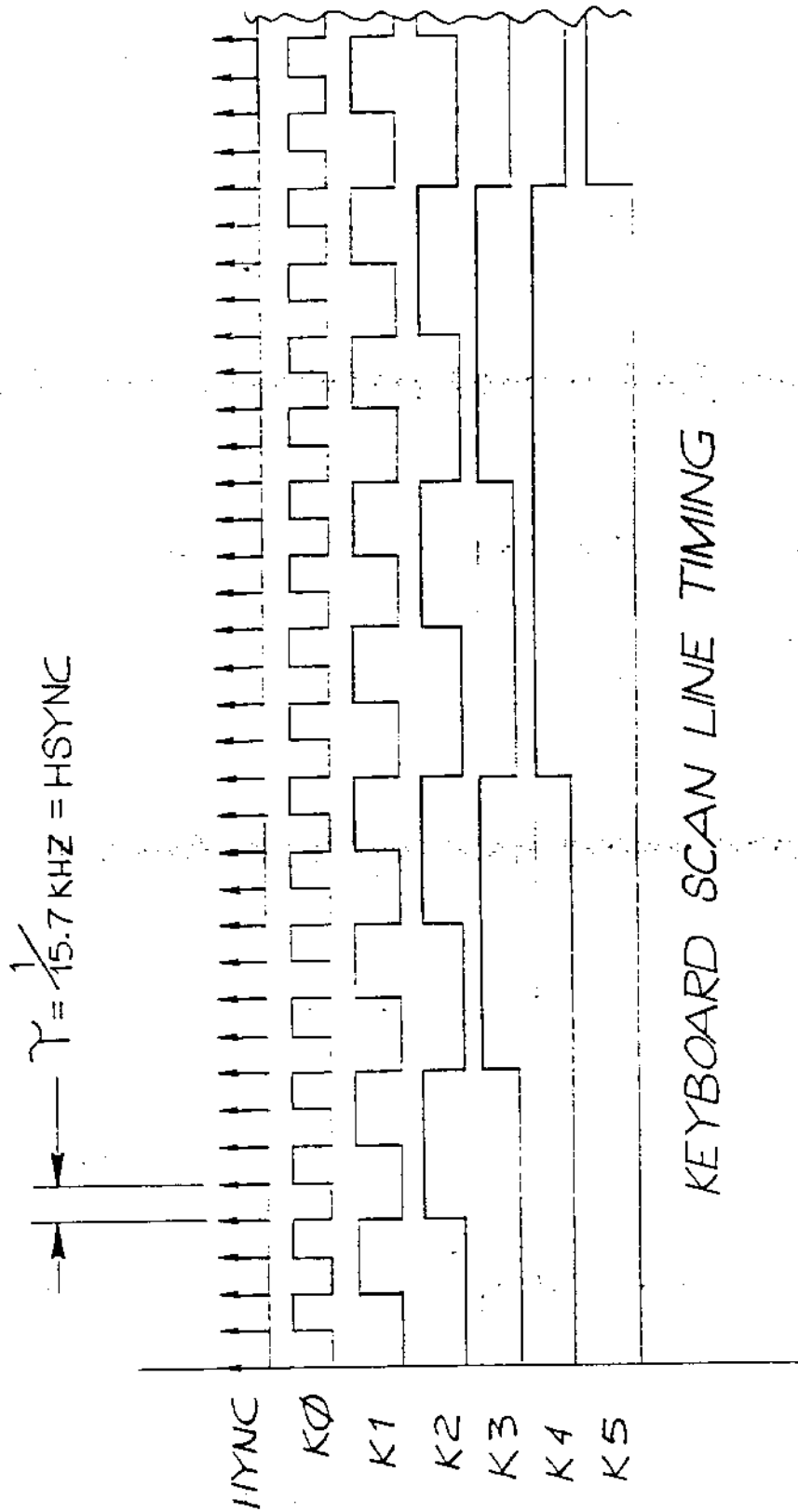
POKEY CHIP

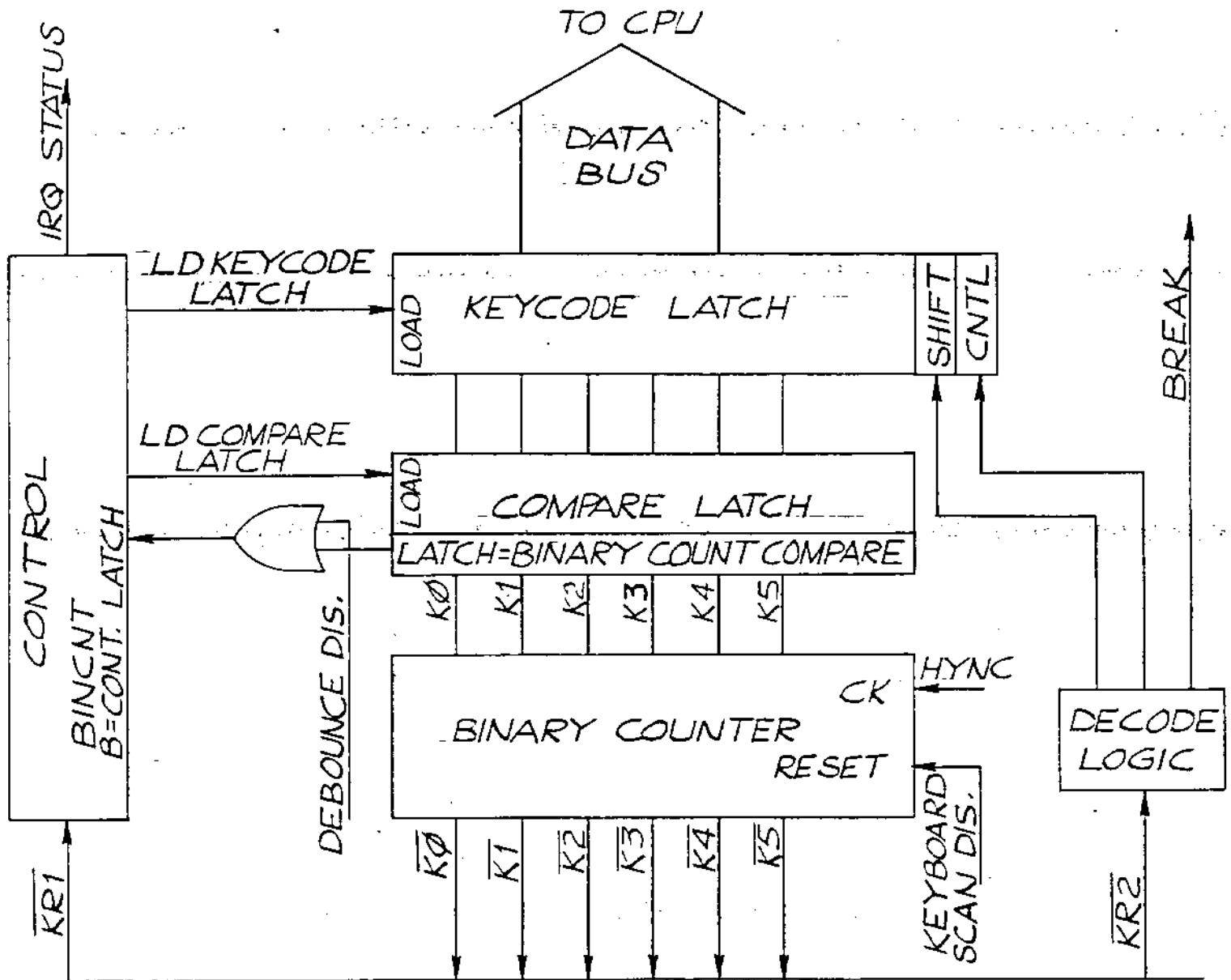
DRAWING NO C012294

REV B

SHEET 12

OF 4





4. POT PORTS

There are eight pot input lines. Each line has a dump transistor and an eight bit latch. There is a binary counter that will count to 228. The counter is reset by strobing POTGO, which also releases the dump transistors. It also starts the binary counter to count once per line. The pot lines now will start to charge. When each line reaches a logic one, it will cause the counter value to be latched into its corresponding latch to be read by the CPU. When the counter reaches 228, the dump transistor is turned back on to pull the pot lines back to ground. The value in the latches will remain until the next POTGO strobe. To operate pot port:

- 1) \$03 → SKCTL ; Turn off init.
- 2) During Vblank service routine, perform the following instructions:
 - A) Read POT0 to POT7 registers
 - B) Write to POTGO register (strobe)

There is an ALLPOT register which allows the logic value of each pot line to be read by the CPU. The main use of Allpot is in the fast scan mode. This is done by:

- 1) Place Pokey in fast scan mode. (SEE SKCTLS)
- 2) Write to POTGO address.
- 3) Wait four cycles of computer clock.
- 4) Now the Allpot register can be read.

NOTE: This address (as well as the fast scan mode) is useful only when the charging capacitors on the P0 - P7 PADS are removed, unless the pads are driven by buffer drivers.

POT0 - POT7 (Pot Values) (00 - 07): These addresses read the value (0 to 228) of 8 pots (paddle controllers) connected to the 8 lines pot port. The paddle controllers are numbered from left to right when facing the console keyboard. Turning the paddle knob clockwise results in decreasing pot values. The values are valid only after 228 TV lines following the "POTGO" command described below or after ALLPOT changes.

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Each Pot Value (0-228)

ALLPOT (All Pot Lines Simultaneously) (08): This address reads the present digital value of the eight line pot port.

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Pot number:

7 6 5 4 3 2 1 0

8 Pot Line States

0 = Pot register value is valid.

1 = Pot register value is not valid.



TITLE

POKEY CHIP

DRAWING NO.

C012294

REV

B

SHEET

15

OF 41

POTGO (Start Pot Scan) (0B):

No
Data Bits Used

This write address starts the pot scan sequence. The pot values (POT0 - POT7) should be read first. This write strobe is then used causing the following sequence:

- 1) Scan Counter cleared to zero.
- 2) Capacitor dump transistors turned off.
- 3) Scan Counter begins counting.
- 4) Counter value captured in each of 8 registers (POT0 - POT7) as each pot line crosses trigger voltage.
- 5) Counter reaches 228, capacitor dump transistors turned on.

5. TIMERS:

Three of the audio channels can be used as timers. Audio channels 1, 2, and 4 are the channels that will cause IRQ interrupts for the timers. If interrupts are enabled, the interrupts will be caused by the audio channel crossing zero. The audio channel divide can be set to their "AUDF" value by strobing STIMER register. By strobing STIMER, the audio outputs are forced to a known state which are logic high for channels 1 and 2, and logic low for channels 3 and 4.

STIMER (Start TIMER) (09):

NOT USED

6. RANDOM NUMBER GENERATOR:

There is a seventeen bit polynomial counter that the CPU can read eight bit of the counter. The polynomial counter can be changed to nine bits by use of AUDCTL. If the Pokey is in the initial state (see SKCTL5), the counter is set to all ones state, therefore, the CPU will read \$FF.

RANDOM (Random Number Generator) (0A): This address reads the high order 8 bits of a 17 bit polynomial counter (9 bit, if bit 7 of AUDCTL = 1).

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



TITLE

POKEY CHIP

DRAWING NO. COL2294

REV B

SHEET 17

OF 4

7. SERIAL PORT

The serial port consists of a serial data output (transmission) line, a serial data input (receiver) line, a serial output clock line, a bi-directional serial data clock line, and other miscellaneous control lines described in the Operating System Manual. Data is transmitted and received as 8 bits of serial data preceded by a logic zero start bit, and succeeded by a logic true stop bit. Input and output clocks are equal to the baud (bit) rate, not 16 times baud rate. Transmitted data changes when the output clock goes true. Received data is sampled when the input clock goes to zero.

Serial Output: The transmission sequence begins when the processor writes 8 bits of parallel data into the serial output register (SEROUT). When any previous data byte transmission is finished the hardware will automatically transfer new data from (SEROUT) to the output shift register; interrupt the processor to indicate an empty (SEROUT) register (ready to be reloaded with the next byte of data), and automatically serially transmit the shift register contents with start-stop bits attached. If the processor responds to the interrupt, and reloads SEROUT before the shift register is completely transmitted, the serial transmission will be smooth and continuous.

Output data is normally transmitted as logic levels (+4V= true, 0V= false). Data can also be transmitted as two tone information. This mode is selected by bit 3 of SKCTL. In this mode audio channel 1 is transmitted in place of logic true, and audio channel 2 in place of logic zero. Channel 2 must be the lower tone of the tone pair.

The processor can force the data output line to zero (or to audio channel 2, if in two tone mode) by setting bit 7 of SKCTL. This is required to force a break (10 zeros) code transmission.

Serial Output Clock: The serial output data always changes when the serial output clock goes true. The clock then returns to zero in the center of the output data bit time.

The baud (bit) rate of the data and clock is determined by audio channel 4 audio channel 2, or by the input clock, depending on the serial mode selected by bits 4, 5, and 6 of SKCTL. (See chart at end of this section.)

Serial Input: The receiving sequence begins when the hardware has received a complete 8 bit serial data word plus start and stop bits. This data is automatically transferred to the 8 bit parallel input register (SERIN), and the processor is interrupted to indicate an input data byte ready to read in SERIN. The processor must



TITLE

POKEY CHIP

DRAWING NO. C012294

REV B

SHEET 18

OF 4

Serial Input (continued)

respond to this interrupt, and read SERIN, before the next input data word reception is complete, otherwise an input data "over-run" will occur. This over-run will be indicated by bit 5 of SKSTAT (if bit 5 of IRQST is not RESET (true) before next input complete), and means input data has been lost. This bit should be tested whenever SERIN is read. Bit 7 of SKSTAT should also be tested to detect frame errors caused by extra (or missing) data bits.

Direct Serial Input: The serial data input line can be read directly by the microprocessor if desired, ignoring the shift register, by reading bit 4 of SKSTAT.

Bi-Directional Clock: This clock line is used to either receive a clock from an external clock source for clocking transmitted or received data, or is used to supply a clock to external devices indicating the transmit or reception rate. This clock line direction is determined by the serial mode selected by bits 4, 5, and 6 of SKCTL. (See mode chart at the end of this section.) Transmitted data changes on the rising edge of this clock. Received data is sampled on the trailing edge of this clock.

Asynchronous Serial Input: Unclocked serial data (at an approximately known (+5%) rate) can be received in the asynchronous modes. The receive (input) shift register is clocked by audio channel 4. Channels 3 and 4 should be used together (AUDCTL bit 3 = 1) for increased resolution. In asynchronous modes, channels 3 and 4 are reset by each start bit at the beginning of each serial data byte. This allows the serial data rate to be slightly different from the rate set by channels 3 and 4.

Serial Mode Control: There are 6 useful modes (of the possible 8) controlled by bits 4, 5, and 6 of SKCTL. These are described on the next page.

Note that two tone output (bit 3 of SKCTL) may be used in any of these modes except for the bottom pair. This is because channel 2 is used to set the output transmit rate and is therefore not available for one of the two tones.

Note that the output clock rate is identical to the output data rate.



TITLE

POKEY CHIP

DRAWING NO

0012294

REV

3

SHEET

19

OF

4

SKCTL (Serial Port Control) (0F): This address writes data into the register that controls the configuration of the serial port, and also the Fast Pot Scan and Keyboard Enable.

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

(Bits perform the functions shown below when true.)

D7 Force Break (force serial output to zero (space))*

D6
D5 \ Serial Port Mode Control (see mode chart on next page).
D4 /

D3 Two Tone (Serial output transmitted as two tone signal instead of logic true/false.)

D2 Fast Pot (Fast Pot Scan. The Pot Scan Counter completes its sequence in two TV line times instead of one frame time. The capacitor dump transistors are completely disabled.)

D1 Enable Key Scan (Enables Keyboard Scanning circuit)

D0 Enable Debounce (Enables Keyboard Debounce circuits)

D0-D1 (Both Zero) Initialize (State used for testing and initializing chip)**

*NOTE: When powered on, serial port output may stay low even if this bit is cleared. To get S. P. high (mark), send a byte out (recommend 00 or FF).

**NOTE: There is no original power on state. Pokey has no reset pin.



TITLE

POKEY CHIP

DRAWING NO.

COL2294

REV

B

SHEET

20

OF

4

Serial Mode Control

Force Break

D7 D6 D5 D4 D3 D2 D1 D0

SKCTL REGISTER

Pot scan and keyboard CTRL

Two Tone Control

Mode Control Bits

A = asynchronous

D6	D5	D4	Out Rate	Out Clock	In Rate	Bi-Dir Clock	Comments
0	0	0	ext	ext	ext	input	Trans. & Receive rates set by external clock. Also internal clock phase reset to zero.
0	0	1	ext	ext	chan 4 A	ext input	Trans. rate set by external clock. Receive asynch. (ch. 4) (CH3 and CH4)
0	1	0	chan 4	chan 4	chan 4	chan 4 output	Trans. & Receive rates set by Chan. 4. Chan. 4 output on Bi-Directional clock line.
0	1	1	CH4 A	CH4 A	CH4 A	input	Not Useful
1	0	0	chan 4	chan 4	ext	ext input	Trans. Rate Set by Chan. 4 Receive Rate set by External Clock.
1	0	1	CH4 A	CH4 A	CH4 A	input	Not Useful
1	1	0	Chan 2	Chan 2	Chan 2	Chan 4 Output	Trans. rate set by chan. 2 Recieve rate set by chan. 4 Chan. 4 out on Bi-Direct. Clock line.
1	1	1	Chan 2	Chan 2	Chan 4 A	Input not used	Trans. Rate set by Chan. 2. Receive asynch. (chan 3&4) Bi-Dir. Clock not used (Tri-state condition)

Two tone (bit3) not useable in these modes

II.27



TITLE

POKEY CHIP

DRAWING NO.

0012294

REV

B

SHEET

21

OF

SKSTAT (Serial Port-Keyboard Status) (0F): This address reads the status register giving information about the serial port and keyboard.

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

(Bits are normally true and provide the following information when zero.)

D7 = 0 = Serial Data Input Frame Error
 D6 = 0 = Keyboard Over-run
 D5 = 0 = Serial Data Input Over-run
 D4 = Serial Input PAD SID Pad
 D3 = 0 = Shift Key Depressed
 D2 = 0 = Last Key is Still Depressed
 D1 = 0 = Serial Input Shift Register Busy
 D0 = 1 Not Used (Logic True)

D5 to D7 latches must be reset to 1 by SKRES.

(D5 and D6 are set to zero when new data and same bit of IRQST is zero.)

SKRES (Reset above Status Register) (0A): This write address resets bits 7, 6, and 5 of the Serial Port-Keyboard Status Register to 1.

not used

SERIN (Serial Input Data) (0D): This address reads the 8 bit parallel holding register that is loaded when a full byte of serial input data has been received. This address is usually read in response to a serial data in interrupt (IRQ and bit 5 of IRQST). Also see IRQEN.

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

SEROUT (Serial Output Data) (0D): This address writes to the 8 bit parallel holding register that is transferred to the output serial shift register when a full byte of serial output data has been transmitted. This address is usually written in response to a serial data out interrupt (IRQ and bit 4 of IRQST).

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

8.) IRQ INTERRUPTS: There are separate IRQ interrupt enable bits for each IRQ interrupt function (bits 0 through 7 of IRQEN). These bits are not initialized by power turn on, and must be initialized by the program before enabling the processor IRQ. The 8 types of IRQ interrupts are:

- D7 = BREAK KEY (depression of the break key)
- D6 = OTHER KEY (depression of any other key)
- D5 = SERIAL INPUT READY (Byte of serial data has been received and is ready to be read by the processor in SERIN register).
- D4 = SERIAL OUTPUT NEEDED (Byte of serial data is being transmitted and SEROUT is ready to be written to again by the processor).
- D3 = TRANSMISSION FINISHED (serial data transmission is finished. Output shift register is empty).
- D2 = TIMER # 4 (audio divider # 4 has counted down to zero)
- D1 = TIMER # 2 (audio divider # 2 has counted down to zero)
- D0 = TIMER # 1 (audio divider # 1 has counted down to zero)

These bits are enabled by bits 0 through 7 of IRQEN and identified by status bits 0 through 7 of IRQST.

The IRQEN register, like the NMEN register, enables interrupts when its bits are 1 (logic true). The IRQST however (unlike the NMIST) has interrupt status bits that are normally logic true, and go to zero to indicate an interrupt request. The IRQST status bits are returned to logic true only by writing a zero into the corresponding IRQEN bit. This will disable the interrupt and simultaneously set the interrupt status bit to one. Bit 3 of IRQST is not a latch and does not get reset by interrupt disable. It is zero when the serial out is empty (out finished) and true when it is not.



TITLE

POKEY CHIP

DRAWING NO. C012294

REV B

SHEET 23

OF 4

IRQST (IRQ Interrupt Status) (0E): This address reads the data from the IRQ Interrupt Status Register.

0 = Interrupt

1 = No Interrupt

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

D7 = 0 Break Key Interrupt

D6 = 0 Other Key Interrupt

D5 = 0 Serial Input Data Ready Interrupt

D4 = 0 Serial Output Data Needed Interrupt

D3 = 0 Serial Output (Byte) Transmission Finished Interrupt *

D2 = 0 Timer 4 Interrupt

D1 = 0 Timer 2 Interrupt

D0 = 0 Timer 1 Interrupt

* - NOTE: Used for generation of 2 stop bits.

IRQEN (IRQ Interrupt Enable) (0E): This address writes data to the IRQ Interrupt Enable bits.

0 = disable, corresponding IRQST bit is set to 1

1 = enable

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

D7 Break Key Interrupt Enable

D6 Other Key Interrupt Enable

D5 Serial Input Data Ready Interrupt Enable

D4 Serial Output Data Needed Interrupt Enable

D3 Serial Out Transmission Finished Interrupt Enable

D2 Timer 4 Interrupt Enable

D1 Timer 2 Interrupt Enable

D0 Timer 1 Interrupt Enable



TITLE

POKEY CHIP

DRAWING NO.

CO12294

REV

B

SHEET

24

OF

4

9. ELECTRICAL PARAMETERS

A. General:

- 1.1 Storage Temperature..... -40°C to $+90^{\circ}\text{C}$
- 1.2 Ambient operating temperature..... 0°C to $+70^{\circ}\text{C}$
- 1.3 Failure rate less than 0.1% per 1000 hours
- 1.4 Maximum voltage range on any pin with respect to VSS
(Pin 1: substrate) without permanent damage to the chip.. -0.5V to $+9.0\text{V}$

B. D.C. and Operating Characteristics:

All voltages are referenced to VSS (pin 1). $T_A = 0^{\circ}\text{C}$ to 70°C .

	MIN.	TYP.	MAX.	UNIT
VCC (PIN 17)	+4.75		+5.25	VOLTS
ICC (PIN 17)			125.0	mA
<u>NORMAL INPUTS:</u>				
SID (PIN 24), CS0 (PIN 30), CS1 (PIN 31), A0-A3 (PIN 36-PIN 33), R/W (PIN 32), KR1 (PIN 25), KR2 (PIN 16)				
V _{IH} INPUT HIGH VOLTAGE:	2.0		VCC	VOLTS
V _{IL} INPUT LOW VOLTAGE:	-0.5		+0.8	VOLTS
I _{LEAKAGE} INPUT LEAKAGE: VIN=7.0 VOLTS			10.0	μA
C _{PIN} PIN CAPACITANCE			7.0	pf
<u>DATA BUS I/O:</u>				
D0-D2 (PIN 38-PIN 40), D3-D7 (PIN 2-PIN 6)				
<u>INPUT:</u>				
V _{IH} INPUT HIGH VOLTAGE:	2.0		VCC	VOLTS
V _{IL} INPUT LOW VOLTAGE:	-0.5		+0.8	VOLTS
I _{LEAKAGE} INPUT LEAKAGE: OUTPUT TRI-STATE VIN=+7.0 VOLTS			10.0	μA
C _{PIN} PIN CAPACITANCE			15.0	pf
<u>OUTPUT:</u>				
V _{OH} OUTPUT HIGH VOLTAGE: I _{LOAD} =-0.1mA	2.4			VOLTS
V _{OL} OUTPUT LOW VOLTAGE: I _{LOAD} =+1.6mA			0.4	VOLTS
C _{LOAD} LOAD CAPACITANCE			130.0	pf



TITLE

POKEY CHIP

DRAWING NO.

CO12294

REV

B

SHEET

25

OF

B.) D.C. and Operating Characteristics: (Continued)

B) D.C. AND OPERATING CHARACTERISTICS: (CONT.)

	MIN.	TYP.	MAX.	UNIT
<u>PI-DIRECTIONAL I/O (SCHMITT TRIGGER INPUT):</u>				
ECLK (PIN 26), P0 (PIN 14), P1 (PIN 15), P2 (PIN 12), P3 (PIN 13), P4 (PIN 10), P5 (PIN 11), P6 (PIN 8), P7 (PIN 9)				
<u>INPUT:</u>				
V _{T+} POSITIVE-GOING THRESHOLD VOLTAGE:	1.9		2.6	VOLTS
V _{T-} NEGATIVE-GOING THRESHOLD VOLTAGE:	1.0		2.1	VOLTS
V _{HYS} HYSTERESIS:	0.3			VOLTS
I _{LEAKAGE} INPUT LEAKAGE: VIN=7.0 VOLTS PULL-DOWN IS TURNED OFF			10.0	uA
C _{PIN} PIN CAPACITANCE			7.0	pf
<u>OUTPUT:</u>				
V _{OL} OUTPUT LOW VOLTAGE: I LOAD=+1.6mA			0.4	VOLTS
C _{LOAD} LOAD CAPACITANCE			30.0	pf
<u>OUTPUT (OPEN DRAIN ONLY):</u>				
IRQ (PIN 29), SDD (PIN 28), OCLK (PIN 27)				
V _{OL} OUTPUT LOW VOLTAGE: I LOAD=+1.6mA			0.4	VOLTS
I _{LEAKAGE} INPUT LEAKAGE: VIN=7.0 VOLTS PULL-DOWN IS TURNED OFF			10.0	uA
C _{LOAD} LOAD CAPACITANCE			30.0	pf
<u>INPUT CLOCK :</u>				
BZ (PIN 7)				
V _{IH} INPUT HIGH VOLTAGE:	2.0		VCC	VOLTS
V _{IL} INPUT LOW VOLTAGE:	-0.5		+0.8	VOLTS
I _{LEAKAGE} INPUT LEAKAGE: VIN=7.0 VOLTS			10.0	uA
C _{PIN} PIN CAPACITANCE			14.0	pf
<u>KEYBOARD SCAN OUTPUT:</u>				
K0-K5 (PIN 23-PIN 18)				
V _{OH} OUTPUT HIGH VOLTAGE: I LOAD=-100.0 uA	2.4			VOLTS
V _{OH} OUTPUT HIGH VOLTAGE: I LOAD=-0.0 uA	4.3			VOLTS
V _{OL} OUTPUT LOW VOLTAGE: I LOAD=+1.6mA			0.4	VOLTS
C _{LOAD} LOAD CAPACITANCE			30.0	pf

D.C. and Operating Characteristics: (Continued)

	MIN.	TYP.	MAX.	UNIT
<u>AUDIO OUTPUT (MULTIPLE OPEN DRAIN OUTPUT):</u>				
AUD (PIN 37)				
V_{OL} OUTPUT LOW VOLTAGE: WITH $10K \pm 5\%$ OHM				
PULL UP TO 4.75 Vdc.				
$\frac{10 \text{ micron}}{10 \text{ micron}}$ DEVICE ON ONLY.			4.2	VOLT
$\frac{20 \text{ micron}}{10 \text{ micron}}$ DEVICE ON ONLY.			3.4	VOLT
$\frac{40 \text{ micron}}{10 \text{ micron}}$ DEVICE ON ONLY.			2.1	VOLT
$\frac{80 \text{ micron}}{10 \text{ micron}}$ DEVICE ON ONLY.			1.2	VOLT
V_{OH} OUTPUT HIGH VOLTAGE: WITH $10K \pm 5\%$ OHM				
PULL UP TO 4.75Vdc AND ALL FOUR DEVICES OFF				
	4.2			VOLT
C_{LOAD} LOAD CAPACITANCE			30.0	pf

C.) Dynamic Operating Characteristics:

(VDD = 5V±5% TA = 0° to 70°C)

Parameter	Note	Signal Type	Symbol	MIN.	MAX.	UNI
<u>INPUT TIMING:</u>						
R/W SETUP TIME		BLE	T _{RWS}	130		nS
R/W HOLD TIME		ATE	T _{RWH}	30		nS
ADDRESS SETUP TIME		BLE	T _{ADS}	130		nS
ADDRESS HOLD TIME		ALE	T _{ADH}	30		nS
CHIP SELECT SETUP TIME		BLE	T _{CSS}	50		nS
CHIP SELECT HOLD TIME		ATE	T _{CSH}	30		nS
DATA SETUP TIME : D0-D7		BTE	T _{DSW}	130		nS
DATA HOLD TIME : D0-D7		ATE	T _{DHW}	10		nS
DATA SETUP TIME : $\overline{KR1}, \overline{KR2},$ P0-P7, SID, BCLK		BTE	T _{DS}	150		nS
<u>OUTPUT TIMING:</u>						
DATA SETUP TIME : D0-D7	2	BTE	T _{DSR}	50		nS
DATA HOLD TIME : D0-D7	2	ATE	T _{DHR}	20		nS
DATA DELAY TIME : $\overline{IRQ}$	1	ALE	T _{DD}		350	nS
DATA DELAY TIME : SOD, BCLK, OCLK	1	ATE	T _{DD}		350	nS
DATA DELAY TIME : AUD	3	ATE	T _{DD}		200	nS
DATA DELAY TIME : $\overline{K0-K5}$	1	ATE	T _{DD}		1.5	uS
DATA DELAY TIME : P0-P7	1	ALE	T _{DD}		1.5	uS

NOTES:

- 1) OUTPUT LOAD AT 30pF + 1 TTL
- 2) OUTPUT LOAD AT 130pF + 1 TTL
- 3) OUTPUT LOAD AT 30pF



TITLE

POKEY CHIP

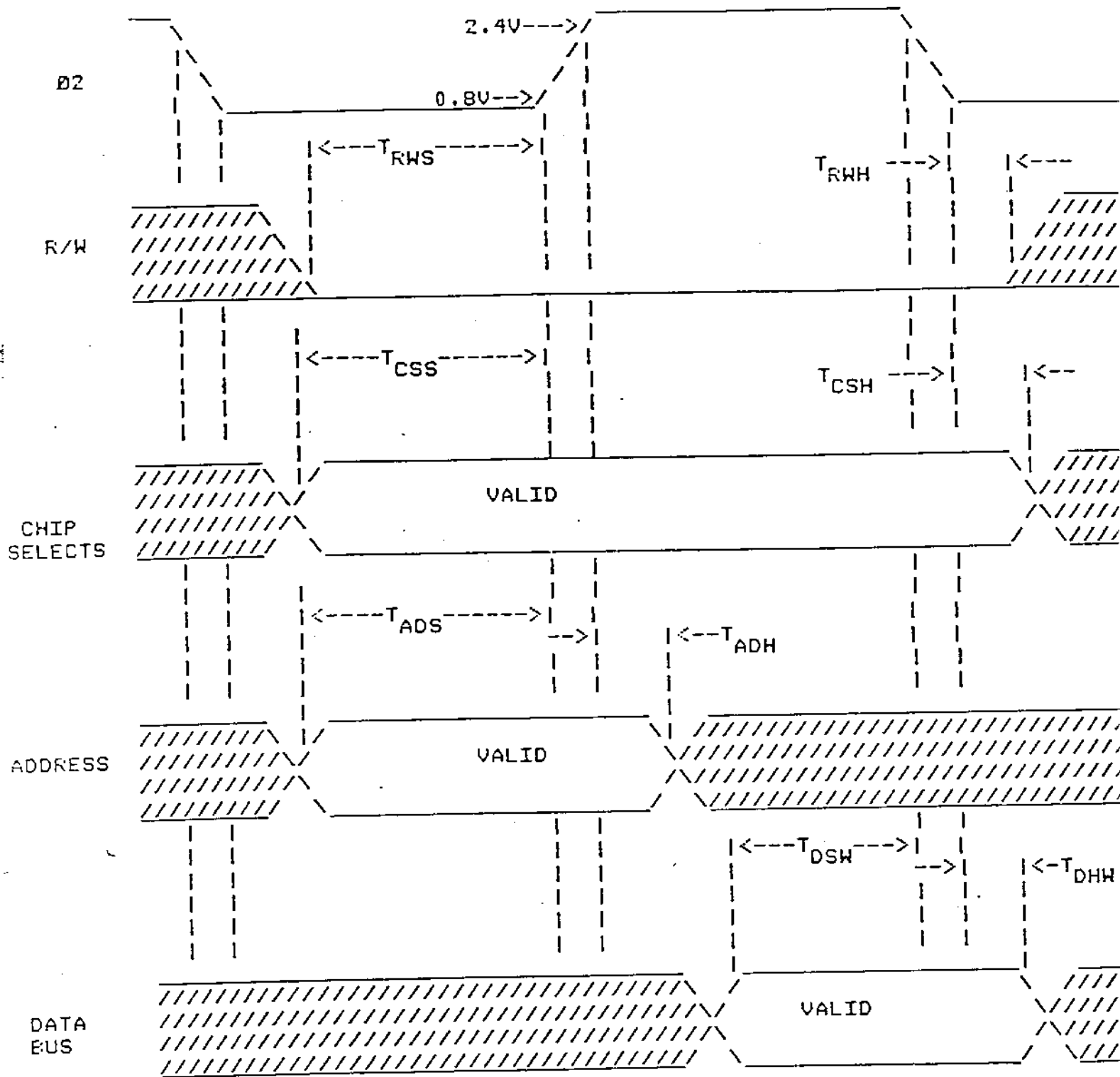
DRAWING NO COL2294

REV B

SHEET 28

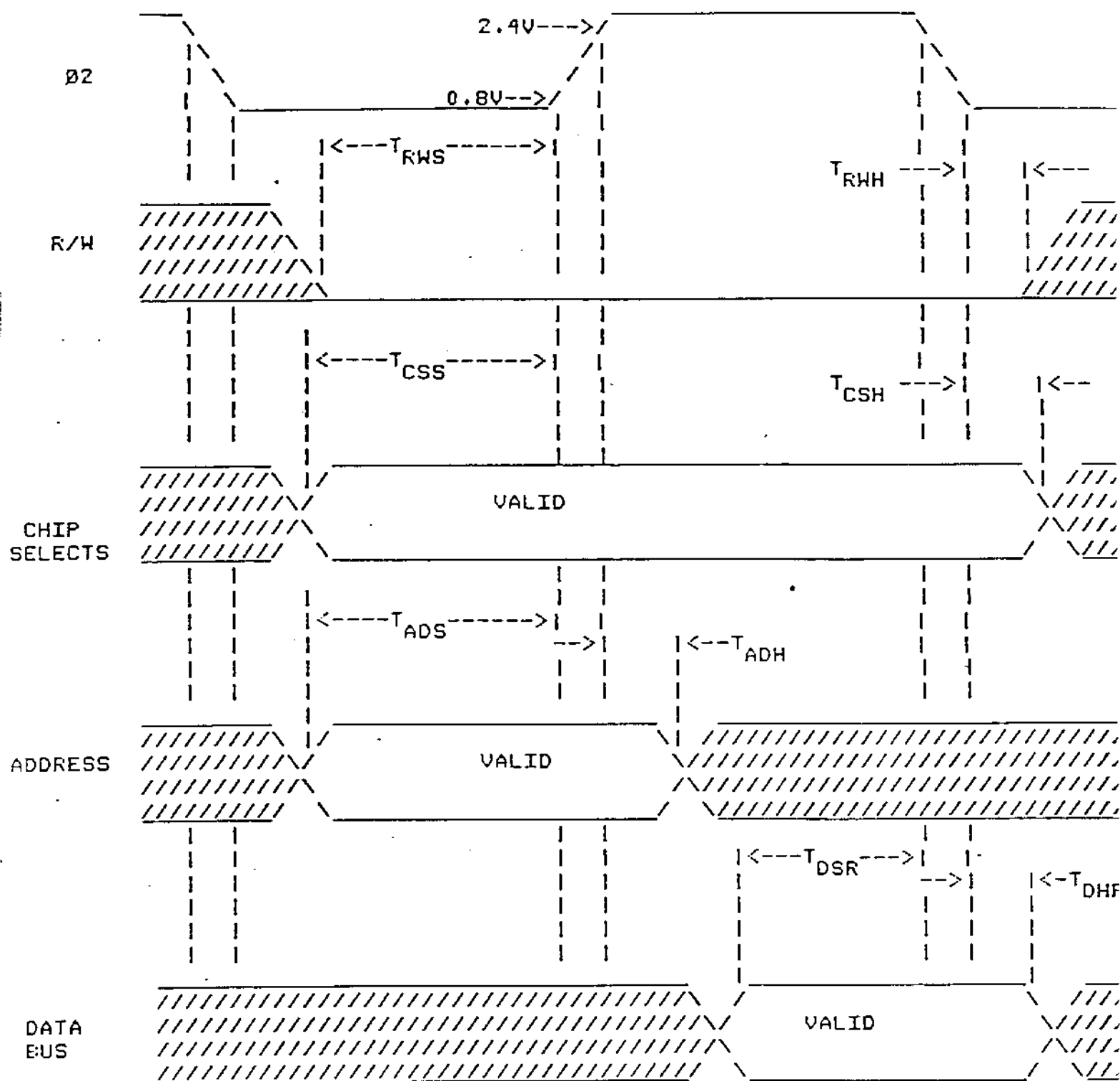
OF

D.) Write I/O Timing:



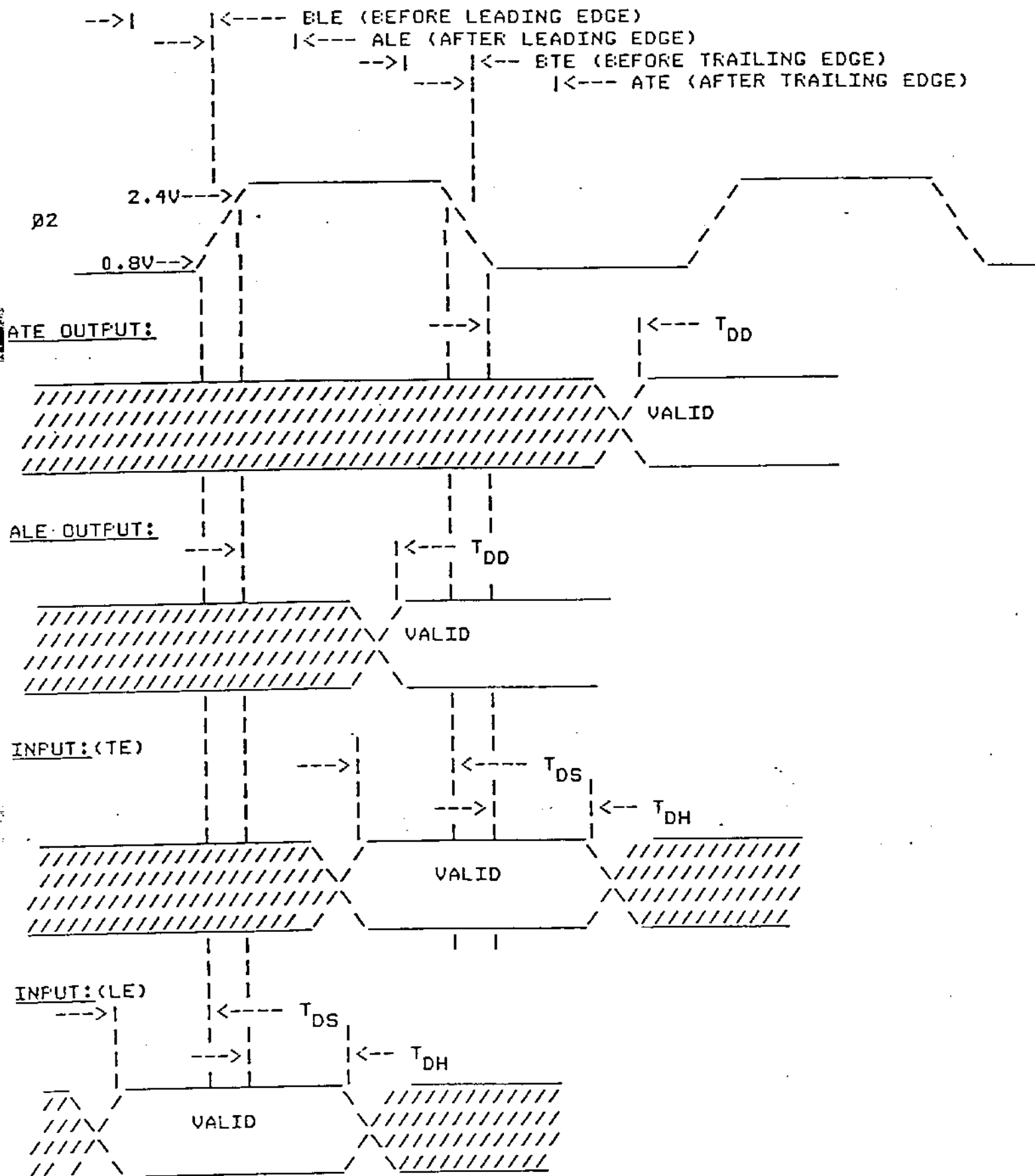
NOTE: ADDRESSES ARE CLOCKED IN ON THE RAISING EDGE OF Ø2.

E.) Read I/O Timing:



NOTE: ADDRESSES ARE CLOCKED IN ON THE RAISING EDGE OF Ø2.

F. I/O Timing:

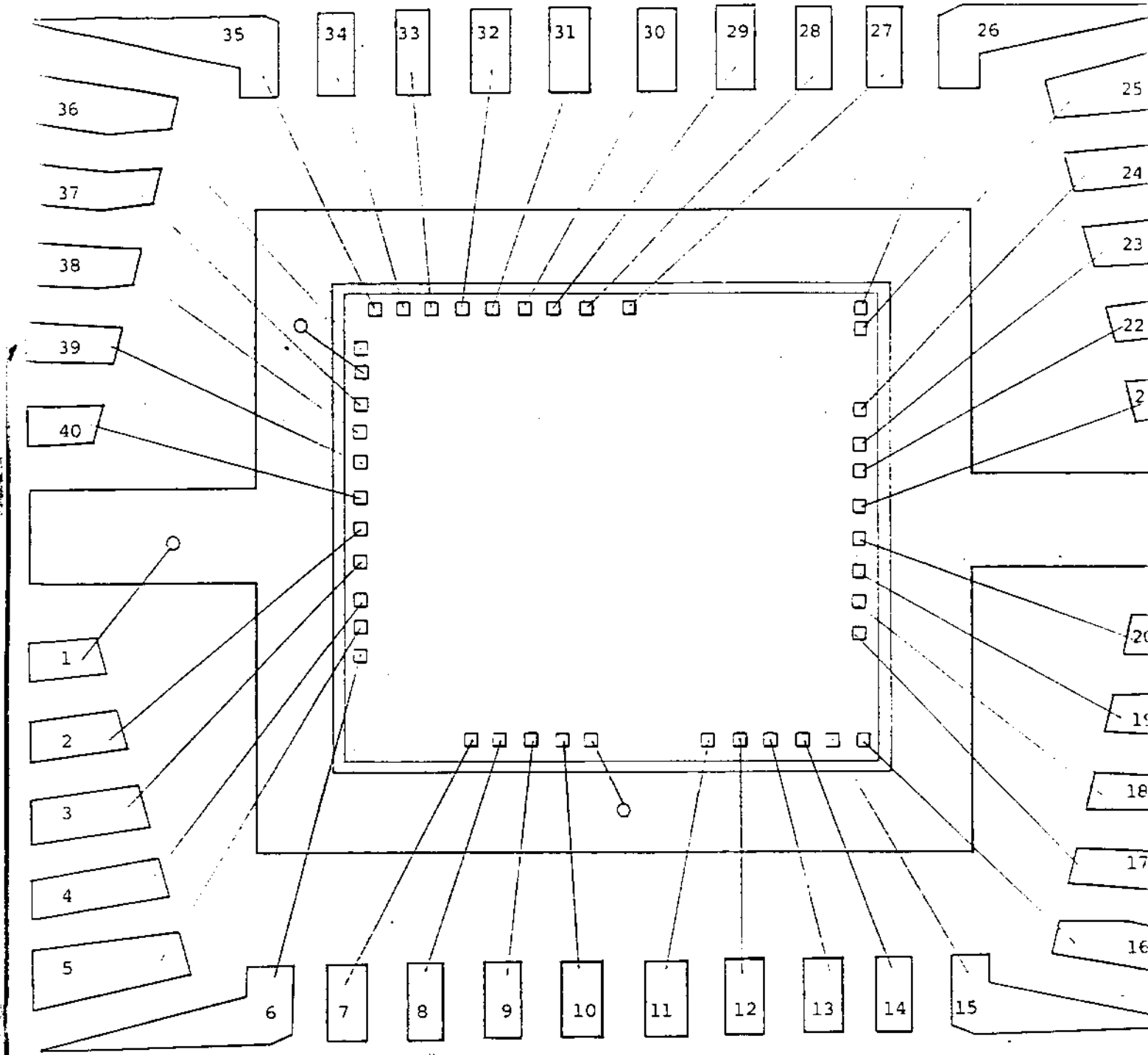


POKEY ADDRESS TABLE:

ADDRESS	WRITE		READ	
	Name	Description	Name	Description
0	AUDF1	Audio Channel 1 Frequency	POT0	Read the value of each pot
1	AUDC1	Audio Channel 1 Control	POT1	
2	AUDF2	Audio Channel 2 Frequency	POT2	
3	AUDC2	Audio Channel 2 Control	POT3	
4	AUDF3	Audio Channel 3 Frequency	POT4	
5	AUDC3	Audio Channel 3 Control	POT5	
6	AUDF4	Audio Channel 4 Frequency	POT6	
7	AUDC4	Audio Channel 4 Control	POT7	
8	AUDCTL	Audio Control	ALLPOT	Read 8 line pot port state
9	STIMER	Start timers	KBCODE	Keyboard code
A	SKRES	Reset Status (SKSTAT)	RANDOM	Random number generator
B	POTGO	Start pot scan sequence		
C				
D	SEROUT	Serial port output register	SERIN	Serial port input register
E	IRQEN	IRQ Interrupt enable	IRQST	IRQ Interrupt status register
F	SKCTLS	Serial port 4 key control	SKSTAT	Serial port 4 key status register

POKEY PIN LIST:

<u>PACKAGE PIN</u>	<u>NAME</u>	<u>FUNCTION</u>	
1	VSS	Ground	I
2	D3	Data Bus	I/O
3	D4	Data Bus	I/O
4	D5	Data Bus	I/O
5	D6	Data Bus	I/O
6	D7	Data Bus	I/O
7	O2	Phase 2 Clock	I
8	P6	Pot Scan	I
9	P7	Pot Scan	I
10	P4	Pot Scan	I
11	P5	Pot Scan	I
12	P2	Pot Scan	I
13	P3	Pot Scan	I
14	P0	Pot Scan	I
15	P1	Pot Scan	I
16	/KR2	Keyboard Scan	I
17	VDD	5 V Power	I
18	/K5	Keyboard Scan	O
19	/K4	Keyboard Scan	O
20	/K3	Keyboard Scan	O
21	/K2	Keyboard Scan	O
22	/K1	Keyboard Scan	O
23	/K0	Keyboard Scan	O
24	SID	Serial Input Data	I
25	/KR1	Keyboard Scan	I
26	BCLK	Bidirection Clock	I/O
27	OCLK	Serial Output Clock	O
28	SOD	Serial Output Data	O
29	/IRQ	Interrupt Request	O
30	/CS0	Chip Select	I
31	CS1	Chip Select	I
32	R/W	Read/Write Control	I
33	A3	Address Bus	I
34	A2	Address Bus	I
35	A1	Address Bus	I
36	A0	Address Bus	I
37	AUDIO	Audio Out	O
38	D0	Data Bus	I/O
39	D1	Data Bus	I/O
40	D2	Data Bus	I/O



SCALE: 20:1
 PACKAGE 204,000-3
 DIE SIZE: 179 mils X 159 mils
 WIRE BOND: 1.1 mil gold T.C.
 DIE ATTACH CAVITY: 210 X 230

COMMENT :
 Six Micron Design Rules.

POKEY BONDING DIAGRAM
 (Figure 11)

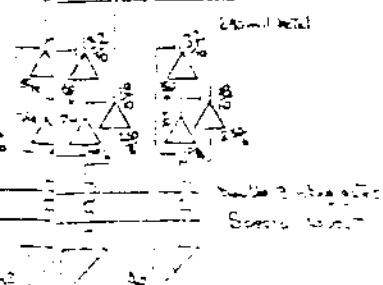
SYM	REVISIONS	DATE	APPROVED
B	SEE SHEET 1		

sheet 34 of 41



POKEY CHIP

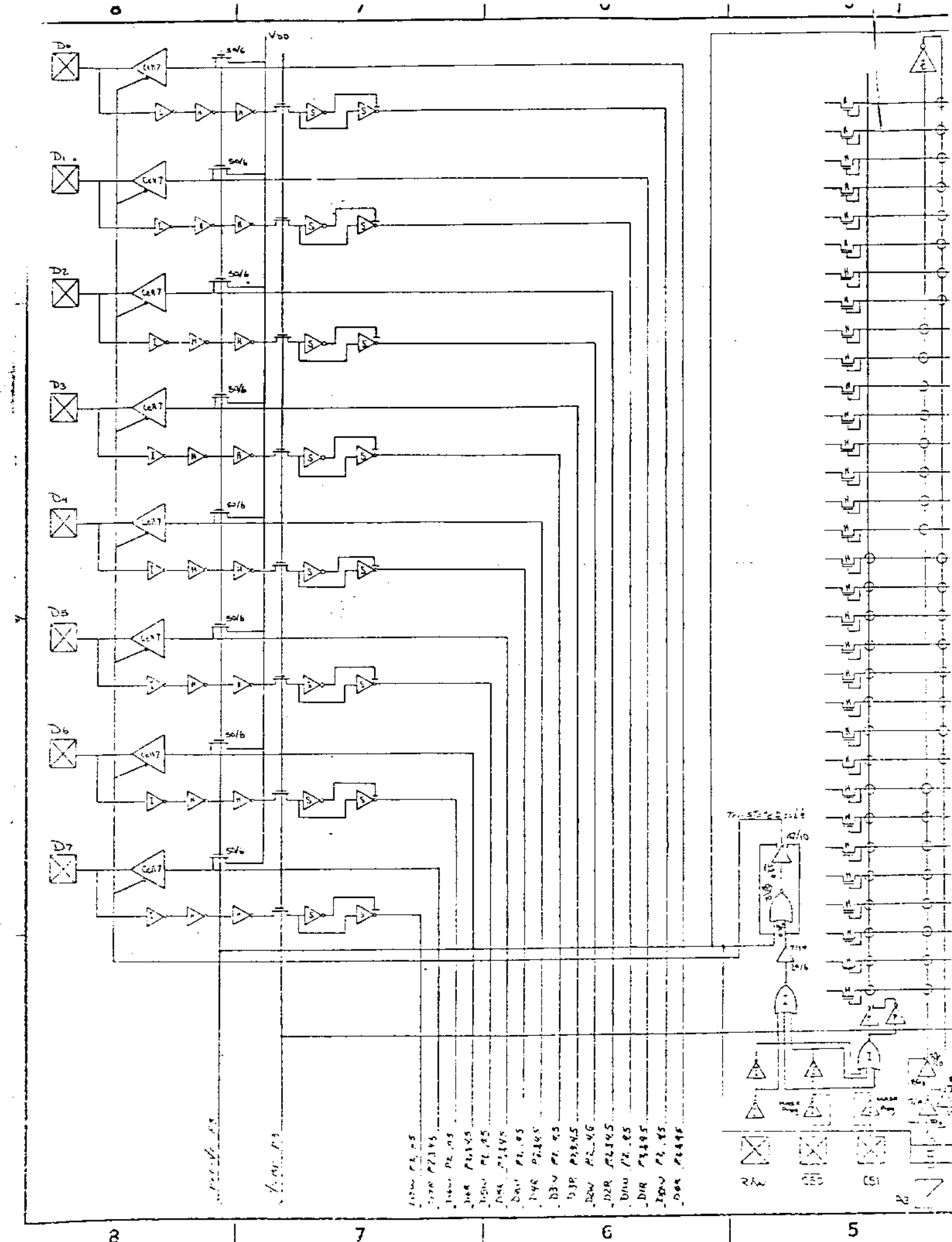
DRAWN BY	ENGINEER, MGR.	MATERIAL
CHECKED	QUAL. ASSURANCE	DRAWING NO.
ENGINEER	MFG ENGINEER	C012994

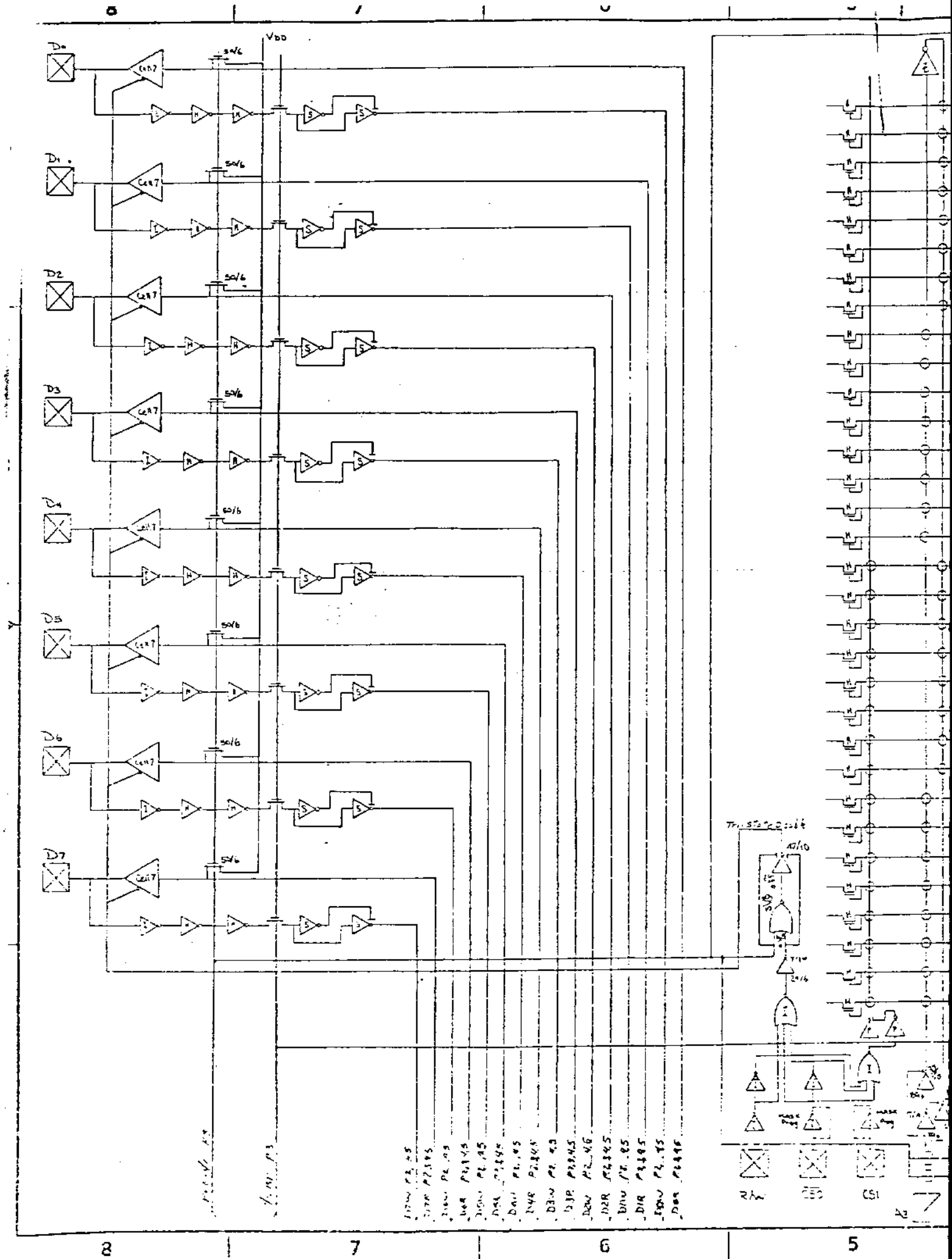
[illegible]

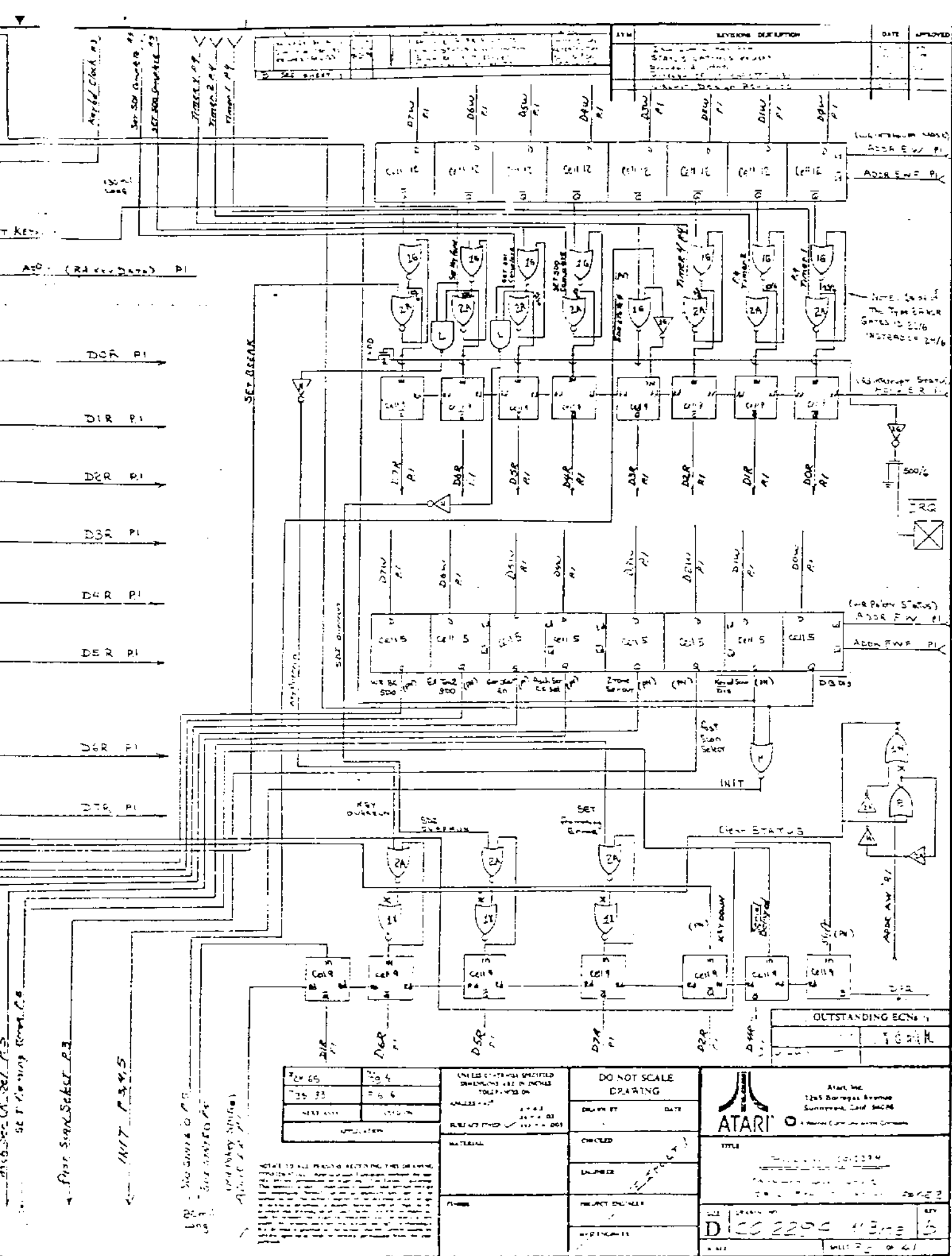
 Atari, Inc.
12055 Boringway Avenue
Sunnyvale, Calif. 94088

PAGE 1

D	002294	447.	(S)
---	--------	------	-----







D
C
B
A

CO12294

36

B

C

B

A

ATARI

1245 Barragans Avenue
Sunnyvale, Calif. 94086

ATARI

CO12294

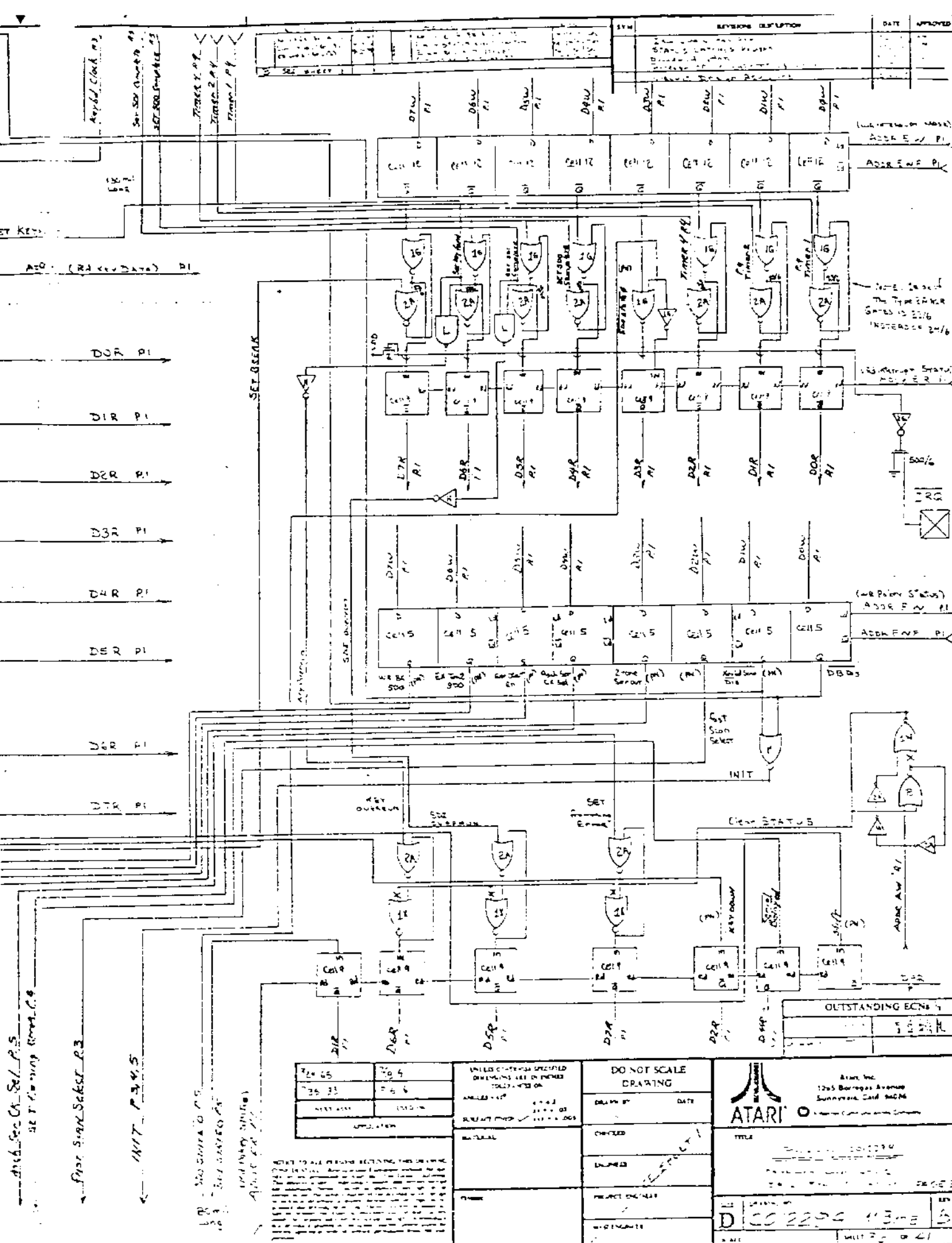
36

B

C

B

A



D
C
B
A

CO12294

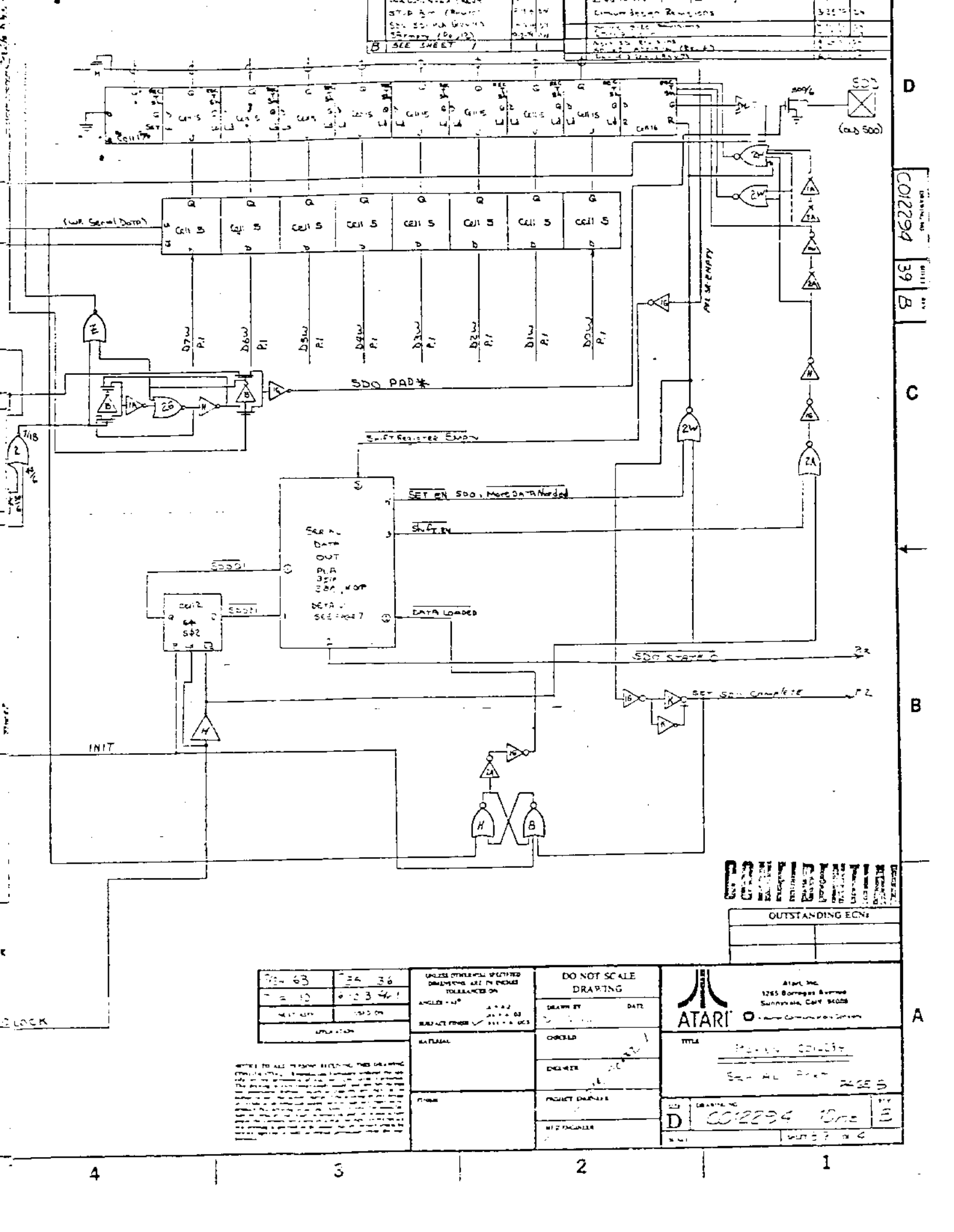
36 B

C

B

A

REVISIONS		DATE		APPROVED	
1.0		1.0		1.0	
2.0		2.0		2.0	
3.0		3.0		3.0	
4.0		4.0		4.0	
5.0		5.0		5.0	
6.0		6.0		6.0	
7.0		7.0		7.0	
8.0		8.0		8.0	
9.0		9.0		9.0	
10.0		10.0		10.0	
11.0		11.0		11.0	
12.0		12.0		12.0	
13.0		13.0		13.0	
14.0		14.0		14.0	
15.0		15.0		15.0	
16.0		16.0		16.0	
17.0		17.0		17.0	
18.0		18.0		18.0	
19.0		19.0		19.0	
20.0		20.0		20.0	
21.0		21.0		21.0	
22.0		22.0		22.0	
23.0		23.0		23.0	
24.0		24.0		24.0	
25.0		25.0		25.0	
26.0		26.0		26.0	
27.0		27.0		27.0	
28.0		28.0		28.0	
29.0		29.0		29.0	
30.0		30.0		30.0	
31.0		31.0		31.0	
32.0		32.0		32.0	
33.0		33.0		33.0	
34.0		34.0		34.0	
35.0		35.0		35.0	
36.0		36.0		36.0	
37.0		37.0		37.0	
38.0		38.0		38.0	
39.0		39.0		39.0	
40.0		40.0		40.0	
41.0		41.0		41.0	
42.0		42.0		42.0	
43.0		43.0		43.0	
44.0		44.0		44.0	
45.0		45.0		45.0	
46.0		46.0		46.0	
47.0		47.0		47.0	
48.0		48.0		48.0	
49.0		49.0		49.0	
50.0		50.0		50.0	
51.0		51.0		51.0	
52.0		52.0		52.0	
53.0		53.0		53.0	
54.0		54.0		54.0	
55.0		55.0		55.0	
56.0		56.0		56.0	
57.0		57.0		57.0	
58.0		58.0		58.0	
59.0		59.0		59.0	
60.0		60.0		60.0	
61.0		61.0		61.0	
62.0		62.0		62.0	
63.0		63.0		63.0	
64.0		64.0		64.0	
65.0		65.0		65.0	
66.0		66.0		66.0	
67.0		67.0		67.0	
68.0		68.0		68.0	
69.0		69.0		69.0	
70.0		70.0		70.0	
71.0		71.0		71.0	
72.0		72.0		72.0	
73.0		73.0		73.0	
74.0		74.0		74.0	
75.0		75.0		75.0	
76.0		76.0		76.0	
77.0		77.0		77.0	
78.0		78.0		78.0	
79.0		79.0		79.0	
80.0		80.0		80.0	
81.0		81.0		81.0	
82.0		82.0		82.0	
83.0		83.0		83.0	
84.0		84.0		84.0	
85.0		85.0		85.0	
86.0		86.0		86.0	
87.0		87.0		87.0	
88.0		88.0		88.0	
89.0		89.0		89.0	
90.0		90.0		90.0	
91.0		91.0		91.0	
92.0		92.0		92.0	
93.0		93.0		93.0	
94.0		94.0		94.0	
95.0		95.0		95.0	
96.0		96.0		96.0	
97.0		97.0		97.0	
98.0		98.0		98.0	
99.0		99.0		99.0	
100.0		100.0		100.0	



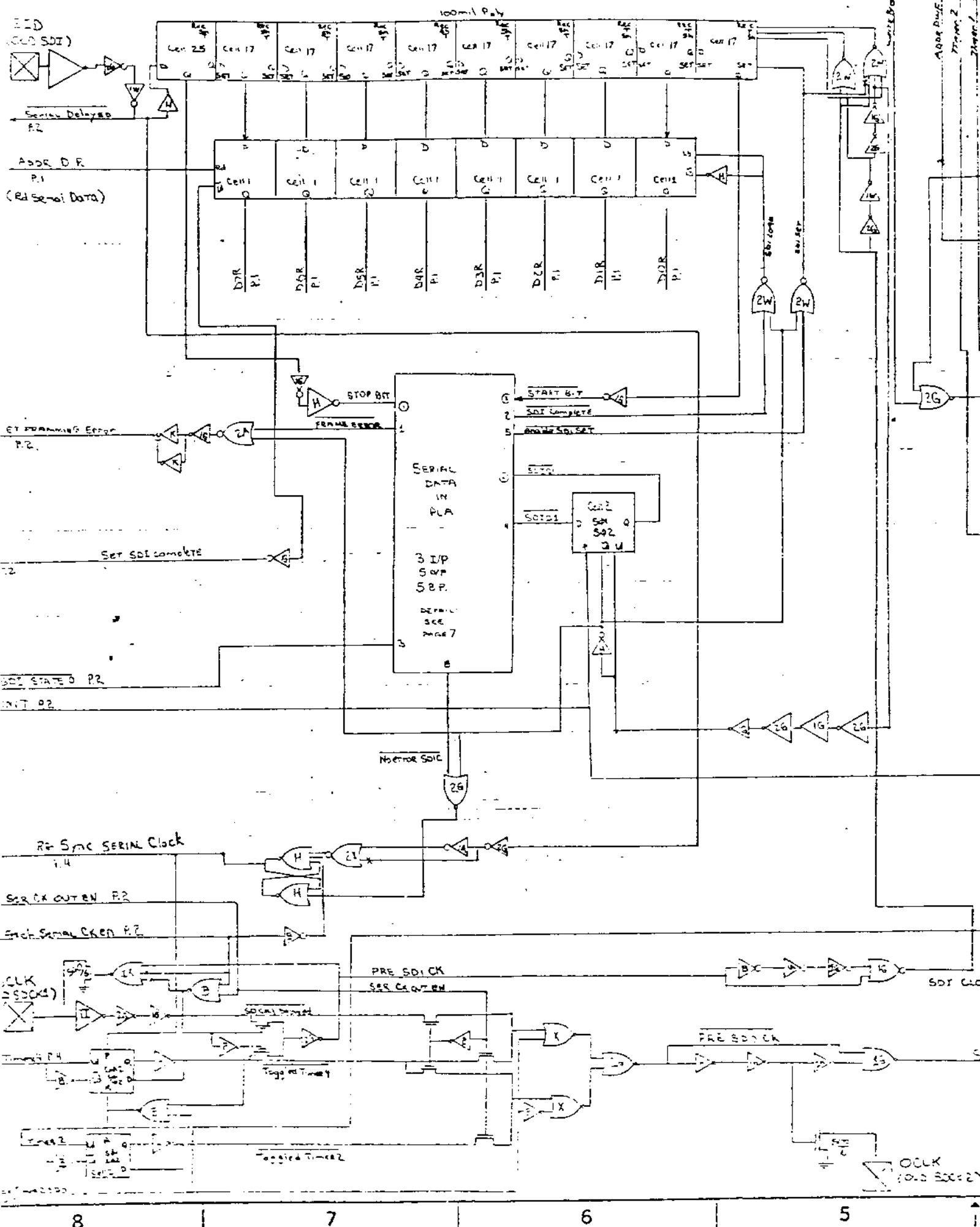
Rev 63	Rev 36
10-10	10-10
10-10	10-10
10-10	10-10

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
ANGLES ±10°
AS SHOWN
SURFACE FINISH
NATURAL
FINISH

DO NOT SCALE DRAWING
DRAWN BY
DATE
CHECKED
DATE
PROJECT ENGINEER
DATE

ATARI 1285 Borregas Avenue Sunnyvale, Calif. 94088	
TITLE Serial Data	
DATE D	DATE 10-10
DRAWN BY E	

NOTICE TO ALL PERSONS RECEIVING THIS DRAWING
THIS DRAWING IS THE PROPERTY OF ATARI INC. AND IS TO BE USED
FOR THE PROJECT AND ONLY FOR THE PROJECT. IT IS NOT TO BE
REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE WRITTEN
CONSENT OF ATARI INC. IT IS TO BE KEPT IN A SAFE PLACE AND
NOT TO BE LOANED TO ANY OTHER PERSON OR ORGANIZATION.
IT IS TO BE DESTROYED WHEN NO LONGER NEEDED FOR THE PROJECT.



100mil PLA

SERIAL DATA IN PLA
3 I/P
5 O/P
5 S/P
DETAILS SEE PAGE 7

Cell 2
2 S/P
2 O/P
+ 2 W

CLK (OLD SDCLK)

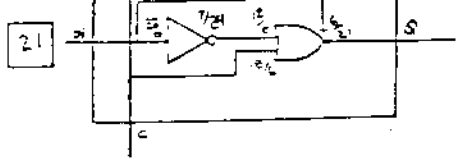
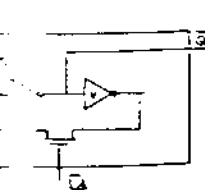
8

7

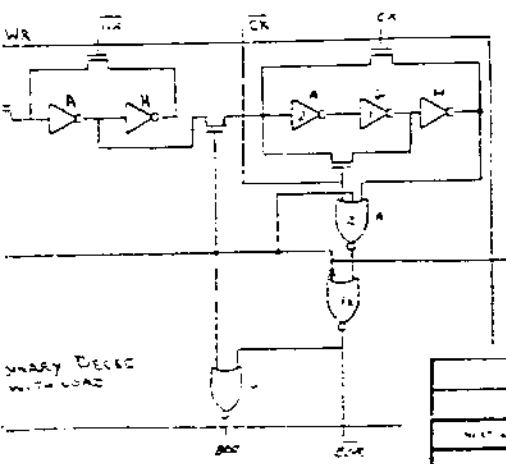
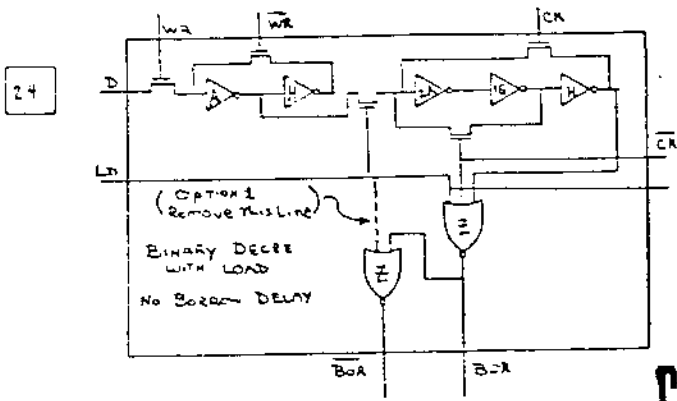
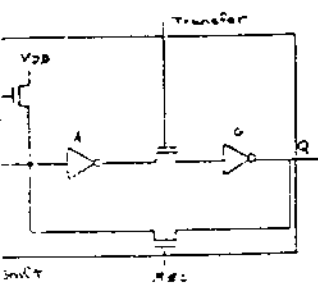
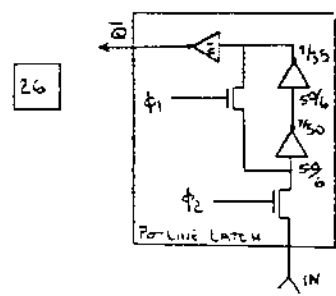
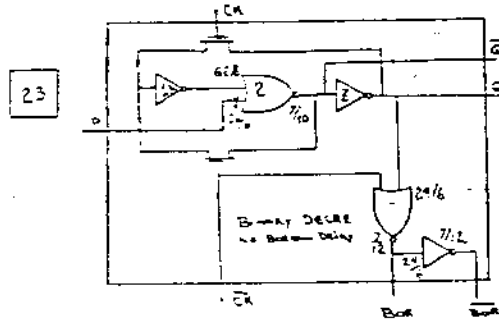
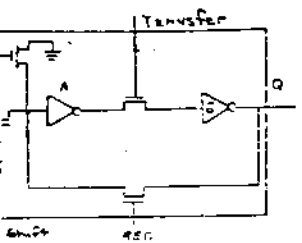
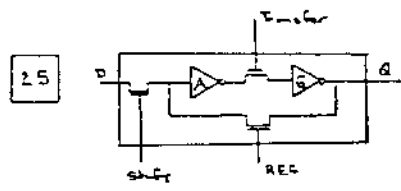
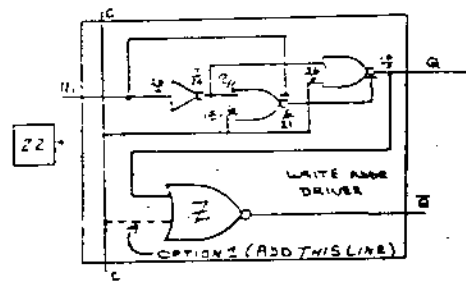
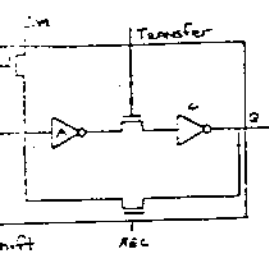
6

5

4



Cells 26,21 (REV B)	7-1-78	24
Cells 2,7,22 (REV A)	5-9-78	24
Cells 3,4,1 (REV B)	5-25-78	24
B SEE SHEET 1		



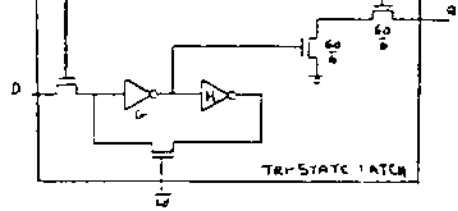
CONTINUED

OUTSTANDING ECNs	

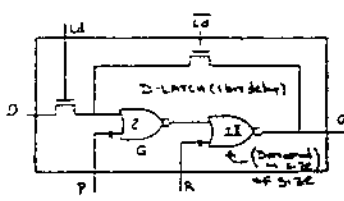
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON ANGLES - 1/2° SURFACE FINISH - 125 ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED		DO NOT SCALE DRAWING DRAWN BY: DATE: CHECKED: DATE: DESIGNED: DATE: APPROVED: DATE: BY: DATE:		ATARI Inc. 1265 Barrington Avenue Sunnyvale, Calif 94086 TITLE: POKEB CELL: 6 PAGE: 6	
MATERIAL:		PART:		D: 1012294 SCALE: 1/8" = 1"	

NOTES TO ALL PERSONS RECEIVING THIS DRAWING
 1. THIS DRAWING IS THE PROPERTY OF ATARI INC.
 2. IT IS TO BE USED FOR THE MANUFACTURE OF THE
 3. PRODUCT DESCRIBED HEREIN ONLY.
 4. IT IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER
 5. WITHOUT THE WRITTEN PERMISSION OF ATARI INC.

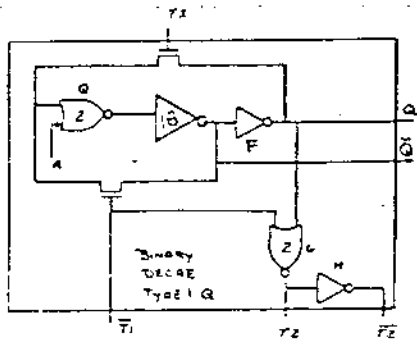
1



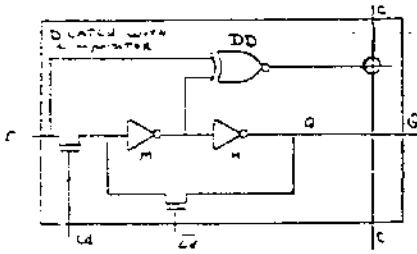
2



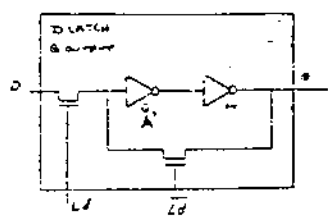
3



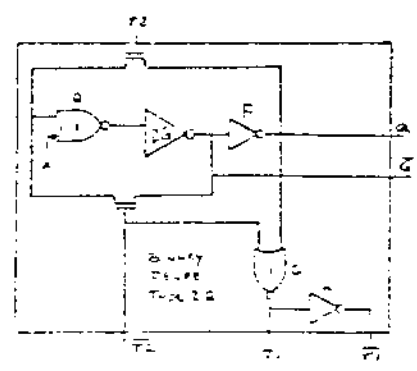
4



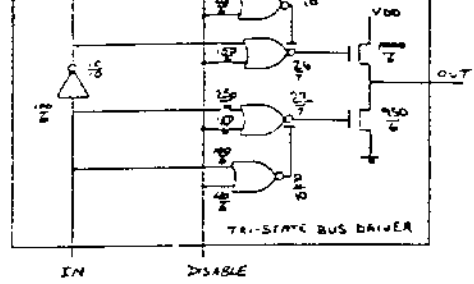
5



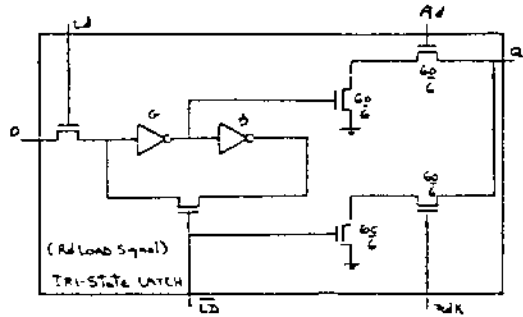
6



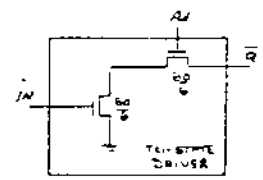
7



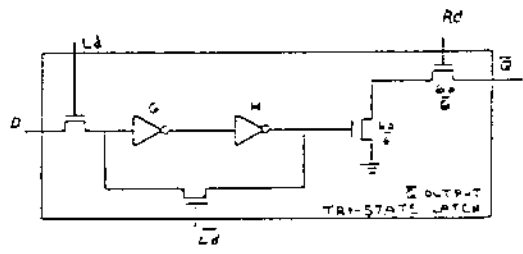
8



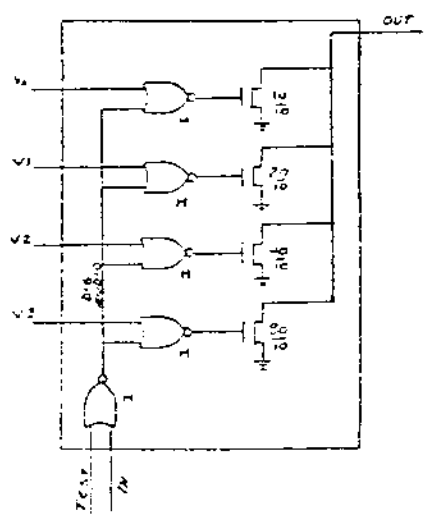
9



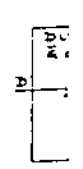
10



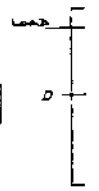
11



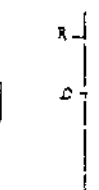
12



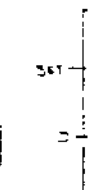
15



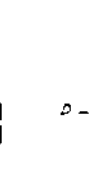
16

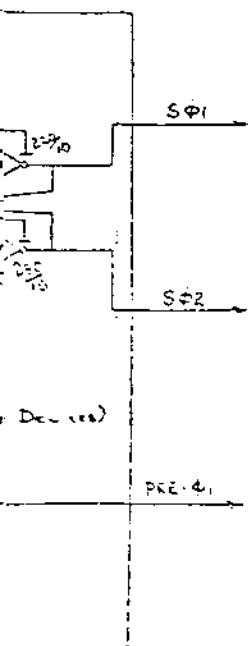
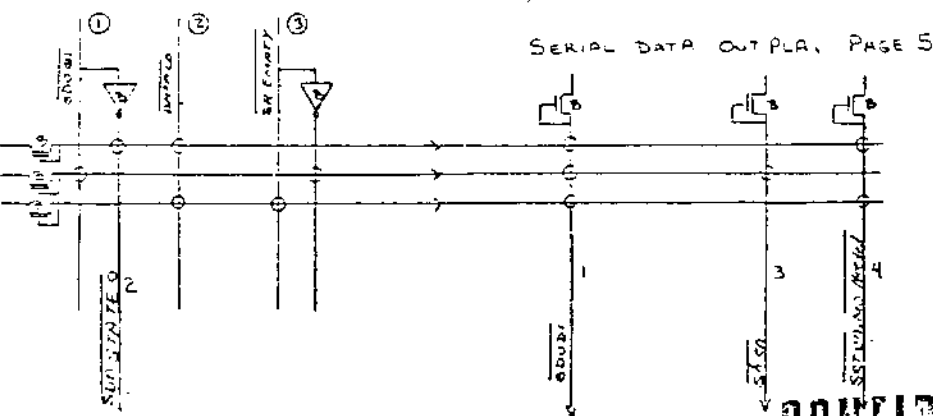


17



18





Keyboard CONTROL PLA ; PAGE 2

SERIAL DATA IN PUA, PAGE 5

SERIAL DATA OUT PLA, PAGE 5

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
84

OUTSTANDING ECNs:

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON		DO NOT SCALE DRAWING		 ATARI, Inc. 1255 Borregas Avenue Sunnyvale, Calif. 94088 - Member Consumer Electronics Company	
AS BUILT	LISTED ON	ANGLES ± 1/2°	± 0.2	DEPTH IN	DATE	TITLE <u>POWER CONDUIT</u> <u>FOR BARNES, INC. 8100</u> <u>DC 229</u>	
APPLICATOR		SURFACE FINISH ✓	± 0.005	CHECKED		DATE <u>11/1/78</u> DRAWN <u>11/1/78</u> PROJECT EST. NO. <u>11/1/78</u> SHEET NUMBER <u>11/1/78</u>	
		MATERIAL				REV. <u>11/1/78</u> DRAWING NO. <u>11/1/78</u> SHEET <u>11/1/78</u> OF <u>11/1/78</u>	
		FINISH					

[illegible]

Alair Inc.
1225 Montgomery Avenue
Springville, Utah 84706

© 2000 Blackwell Science Ltd *Journal of Internal Medicine* 247: 395–402

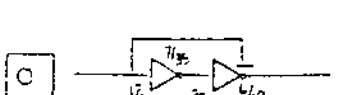
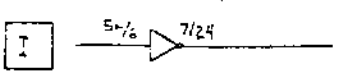
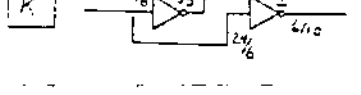
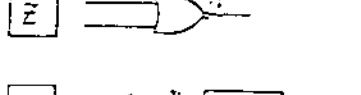
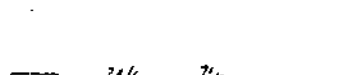
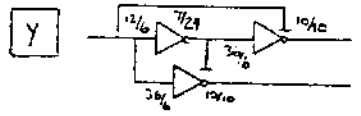
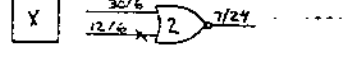
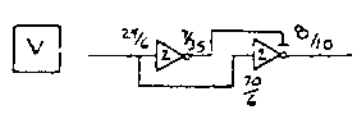
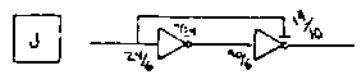
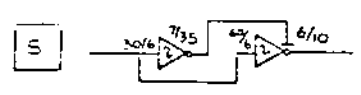
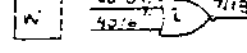
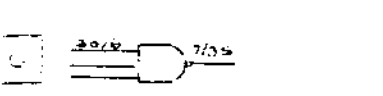
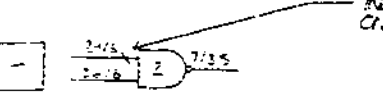
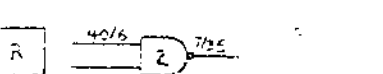
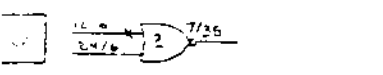
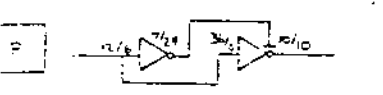
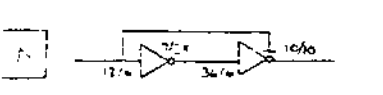
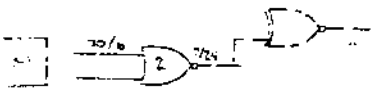
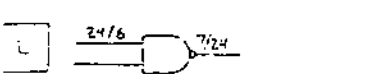
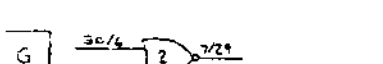
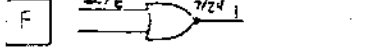
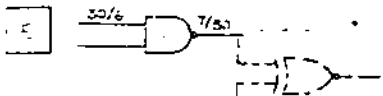
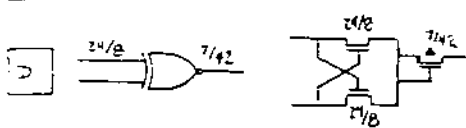
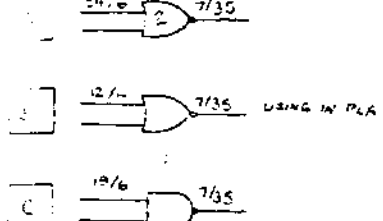
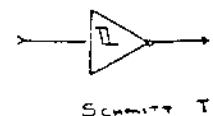
1992 10 24

Page 7

DATE: 03/22/94

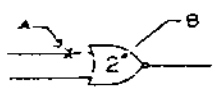
118

2511	م. ف.
------	-------



INDICATES NO COUPLER ON THIS INPUT.

NOTE:



A X INDICATES NO COUPLER ON THAT INPUT.
B NUMBER INDICATES CLOCK PHASE OF INPUT COUPLERS.

